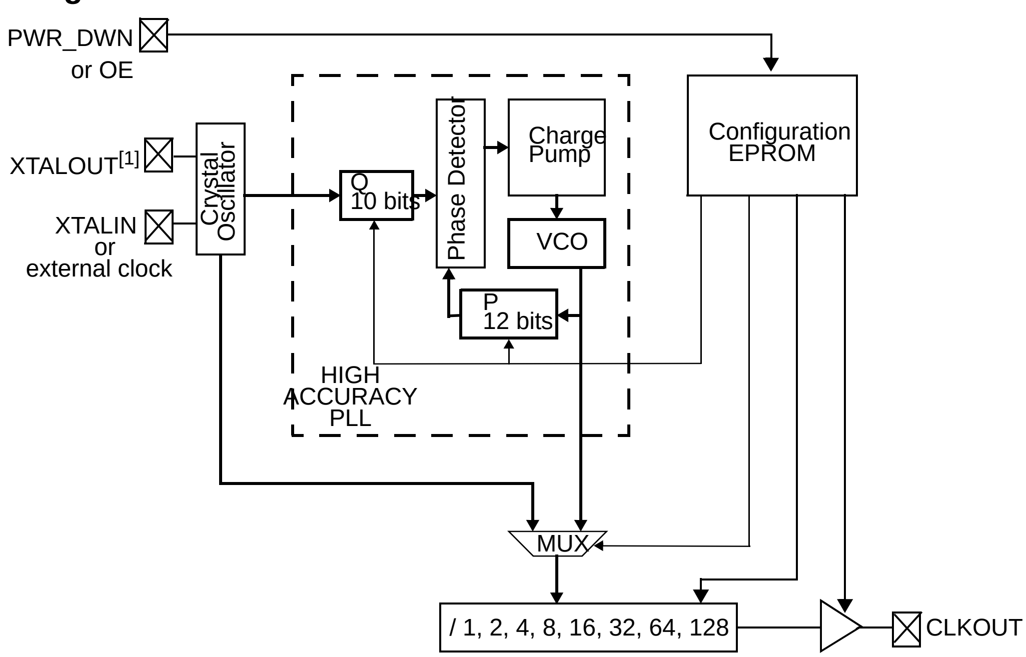
CY2077

High-accuracy EPROM Programmable Single-PLL Clock Generator

Features

- High-accuracy PLL with 12-bit multiplier and 10-bit divider
- EPROM programmability
- 3.3 V or 5 V operation
- Operating frequency
  - 390 kHz–133 MHz at 5 V
  - 390 kHz–100 MHz at 3.3 V
- Reference input from either a 10–30 MHz fundamental toned crystal or a 1–75 MHz external clock
- EPROM selectable TTL or CMOS duty cycle levels
- Sixteen selectable post-divide options, using either PLL or reference oscillator/external clock
- Programmable PWR_DWN or OE pin, with asynchronous or synchronous modes
- Low jitter outputs typically
  - 80 ps at 3.3 V/5 V
- Controlled rise and fall times and output slew rate
- Available in both commercial and industrial temperature ranges
- Factory programmable device options

Logic Block Diagram



Note
1. When using an external clock source, leave XTALOUT floating.

Contents

Pinouts

Figure 1. Pin Diagram - 8 Pin Top View

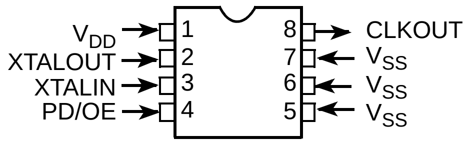


Table 1. Pin Definition - 8 Pin

Pin Name	Pin #	Pin Description
V_{DD}	1	Voltage supply
V_{SS}	5,6,7	Ground (all the pins must be grounded)
X_D	2	Crystal output (leave this pin floating when external reference is used)
X_G	3	Crystal input or external input reference
PWR_DWN / OE	4	EPROM programmable power down or output enable pin. PWR_DWN is active low. OE is active high. Weak pull up.
CLKOUT	8	Clock output. Weak pull down

Functional Description

CY2077 is an EPROM-programmable, high-accuracy, general-purpose, PLL-based design for use in applications such as modems, disk drives, CD-ROM drives, video CD players, DVD players, games, set-top boxes, and data/telecommunications.

CY2077 can generate a clock output up to 133 MHz at 5 V or 100 MHz at 3.3 V. It has been designed to give the customer a very accurate and stable clock frequency with little to zero PPM error. CY2077 contains a 12-bit feedback counter divider and 10-bit reference counter divider to obtain a very high resolution to meet the needs of stringent design specifications. Furthermore, there are eight output divide options of /1, /2, /4, /8, /16, /32, /64, and /128. The output divider can select between the PLL and crystal oscillator output/external clock, providing a total of 16 different options to add more flexibility in designs. TTL or CMOS duty cycles can be selected.

Power management with the CY2077 is also very flexible. The user can choose either a PWR_DWN, or an OE feature with which both have integrated pull up resistors. PWR_DWN and OE signals can be programmed to have asynchronous and synchronous timing with respect to the output signal. There is a weak pull down on the output that pulls CLKOUT LOW when either the PWR_DWN or OE signal is LOW. This weak pull down can easily be overridden by another clock signal in designs where multiple clock signals share a signal path.

Multiple options for output selection, better power distribution layout, and controlled rise and fall times enable the CY2077 to be used in applications that require low jitter and accurate reference frequencies.

EPROM Configuration Block

Table 2. EPROM Adjustable Features

EPROM Adjustable Features	
Adjust Freq.	Feedback counter value (P)
	Reference counter value (Q)
	Output divider selection
Duty cycle levels (TTL or CMOS)	
Power management mode (OE or PWR_DWN)	
Power management timing (synchronous or asynchronous)	

PLL Output Frequency

CY2077 contains a high-resolution PLL with 12-bit multiplier and 10-bit divider.[2] The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \bullet (P+5)}{(Q+2)} \bullet F_{REF}$$

where P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

The calculation of P and Q values for a given PLL output frequency is handled by the CyberClocks™ software. Refer to "“Programming Procedures” on page 13” for details.

Note

2. When using CyClocks, note that the PLL frequency range is from 50 MHz to 250 MHz for 5 V V_{DD} supply, and 50 MHz to 180 MHz for 3 V V_{DD} supply. The output frequency is determined by the selected output divider.

Power Management Features

PWR_DWN and OE options are configurable by EPROM programming for the CY2077. In PWR_DWN mode, all active circuits are powered down when the control pin is set LOW. When the control pin is set back HIGH, both the PLL and oscillator circuit must relock. In the case of OE, the output is three-stated and weakly pulled down when the control pin is set LOW. The oscillator and PLL are still active in this state, which leads to a quick clock output return when the control pin is set back HIGH.

Additionally, PWR_DWN and OE can be configured to occur asynchronously or synchronously with respect to CLKOUT. In asynchronous mode, PWR_DWN or OE disables CLKOUT immediately (allowing for logic delays), without respect to the current state of CLKOUT. Synchronous mode prevents output glitches by waiting for the next falling edge of CLKOUT after PWR_DWN, or OE becomes asserted. In either asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of CLKOUT.

Table 3. Device Functionality: Output Frequencies

Symbol	Description	Condition	Min	Max	Unit
Fo	Output frequency	V_{DD} = 4.5–5.5 V	0.39	133	MHz
		V_{DD} = 3.0–3.6 V	0.39	100	MHz

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage .... –0.5 to +7.0 V

Input voltage .... –0.5 V to V_{DD} +0.5 V

Storage temperature (non-condensing)...... –55°C to +150°C

Junction temperature... 150°C

Static discharge voltage... $\geq$ 2000 V (per MIL-STD-883, method 3015)

Operating Conditions for Commercial Temperature Device

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	5.5	V
T_A	Operating temperature, ambient	0	+70	°C
C_{TTL}	Max. capacitive load on outputs for TTL levels V_{DD} = 4.5 – 5.5 V, output frequency = 1 – 40 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 40 – 125 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 125 – 133 MHz	 – – –	 50 25 15	 pF pF pF
C_{CMOS}	Max. capacitive load on outputs for CMOS levels V_{DD} = 4.5 – 5.5 V, output frequency = 1 – 40 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 40 – 125 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 125 – 133 MHz V_{DD} = 3.0 – 3.6 V, output frequency = 1 – 40 MHz V_{DD} = 3.0 – 3.6 V, output frequency = 40 – 100 MHz	 – – – – –	 50 25 15 30 15	 pF pF pF pF pF
X_{REF}	Reference frequency, input crystal with C_{load} = 10 pF	10	30	MHz
	Reference frequency, external clock source	1	75	MHz
t_{PU}	Power up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

T_A = 0°C to +70°C

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	V_{DD} = 4.5 – 5.5 V V_{DD} = 3.0 – 3.6 V	– –	– –	0.8 0.2 V_{DD}	V V
V_{IH}	High-level input voltage	V_{DD} = 4.5 – 5.5 V V_{DD} = 3.0 – 3.6 V	2.0 0.7 V_{DD}	– –	– –	V V
V_{OL}	Low-level output voltage	V_{DD} = 4.5 – 5.5 V, I_{OL}= 16 mA V_{DD} = 3.0 – 3.6 V, I_{OL}= 8 mA	– –	– –	0.4 0.4	V V
V_{OHCMOS}	High-level output voltage CMOS levels	V_{DD} = 4.5 – 5.5 V, I_{OH}= –16 mA V_{DD} = 3.0 – 3.6 V, I_{OH}= –8 mA	V_{DD} – 0.4 V_{DD} – 0.4	– –	– –	V V
V_{OHTTL}	High-level output voltage TTL levels	V_{DD} = 4.5 – 5.5 V, I_{OH}= –8 mA	2.4	–	–	V
I_{IL}	Input low current	V_{IN} = 0 V	–	–	10	µA
I_{IH}	Input high current	V_{IN} = V_{DD}	–	–	5	µA
I_{DD}	Power supply current Unloaded	V_{DD} = 4.5 – 5.5 V, output frequency <= 133 MHz V_{DD} = 3.0 – 3.6 V, output frequency <= 100 MHz	– –	– –	45 25	mA mA
I_{DDS}[3]	Stand-by current (PD = 0)	V_{DD} = 4.5 – 5.5 V V_{DD} = 3.0 – 3.6 V	– –	25 10	100 50	µA µA
R_{UP}	Input pull up resistor	V_{DD} = 4.5 – 5.5 V, V_{IN} = 0 V V_{DD} = 4.5 – 5.5 V, V_{IN} = 0.7 V_{DD}	1.1 50	3.0 100	8.0 200	MΩ kΩ
I_{OE_CLKOUT}	CLKOUT pull down current	V_{DD} = 5.0	–	20	–	µA

Note

3. If external reference is used, it is required to stop the reference (set reference to LOW) during power down.

Output Clock Switching Characteristics Commercial

Over the Operating Range[4]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_{1w}	Output duty cycle at 1.4 V, V_{DD} = 4.5 – 5.5 V $t_{1w} = t_{1A} \div t_{1B}$	1 – 40 MHz, C_L <= 50 pF 40 – 125 MHz, C_L <= 25 pF 125 – 133 MHz, C_L <= 15 pF	45 45 45	– – –	55 55 55	% % %
t_{1x}	Output duty cycle at V_{DD}/2, V_{DD} = 4.5 – 5.5 V $t_{1x} = t_{1A} \div t_{1B}$	1 – 40 MHz, C_L <= 50 pF 40 – 125 MHz, C_L <= 25 pF 125 – 133 MHz, C_L <= 15 pF	45 45 45	– – –	55 55 55	% % %
t_{1y}	Output duty cycle at V_{DD}/2, V_{DD} = 3.0 – 3.6 V $t_{1y} = t_{1A} \div t_{1B}$	1 – 40 MHz, C_L <= 30 pF 40 – 100 MHz, C_L <= 15 pF	45 40	– –	55 60	% %
t_2	Output clock rise time	Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 50 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 25 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 15 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 4.5 V – 5.5 V, C_L = 50 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 30 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 15 pF	– – – – – –	– – – – – –	1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_3	Output clock fall time	Between 0.8 V –2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 50 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 25 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 15 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 4.5 V – 5.5 V, C_L = 50 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 30 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 15 pF	– – – – – –	– – – – – –	1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_4	Startup time out of power down	PWR_DWN pin LOW to HIGH[5]	–	1	2	ms
t_{5a}	Power down delay time (synchronous setting)	PWR_DWN pin LOW to output LOW (T= period of output CLK)	–	T/2	T + 10	ns
t_{5b}	Power down delay time (asynchronous setting)	PWR_DWN pin LOW to output LOW	–	10	15	ns
t_6	Power up time	From power on[5]	–	1	2	ms
t_{7a}	Output disable time (synchronous setting)	OE pin LOW to output high-Z (T= period of output CLK)	–	T/2	T + 10	ns
t_{7b}	Output disable time (asynchronous setting)	OE pin LOW to output high-Z	–	10	15	ns
t_8	Output enable time (always synchronous enable)	OE pin LOW to HIGH (T= period of output CLK)	–	T	1.5T+ 25ns	ns
t_9	Peak-to-peak period jitter	V_{DD} = 3.0 V – 3.6 V, 4.5 V – 5.5 V, Fo > 33 MHz, V_{CO} > 100 MHz V_{DD} = 3.0 V – 5.5 V, Fo < 33 MHz	– –	80 0.3%	150 1%	ps % of F_O

Notes
4. Not all parameters measured in production testing.
5. Oscillator start time can not be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70Ω.

Operating Conditions for Industrial Temperature Device

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	5.5	V
T_A	Operating temperature, ambient	–40	+85	°C
C_{TTL}	Max. capacitive load on outputs for TTL levels V_{DD} = 4.5 – 5.5 V, output frequency = 1 – 40 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 40 – 125 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 125 – 133 MHz	 – – –	 35 15 10	 pF pF pF
C_{CMOS}	Max. capacitive load on outputs for CMOS levels V_{DD} = 4.5 – 5.5 V, output frequency = 1 – 40 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 40 – 125 MHz V_{DD} = 4.5 – 5.5 V, output frequency = 125 – 133 MHz V_{DD} = 3.0 – 3.6 V, output frequency = 1 – 40 MHz V_{DD} = 3.0 – 3.6 V, output frequency = 40 – 100 MHz	 – – – – –	 35 15 10 20 10	 pF pF pF pF pF
X_{REF}	Reference frequency, input crystal with C_{load} = 10 pF	10	30	MHz
	Reference frequency, external clock source	1	75	MHz
t_{PU}	Power up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

T_A = –40°C to +85°C

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	V_{DD} = 4.5 – 5.5 V V_{DD} = 3.0 – 3.6 V	– –	– –	0.8 0.2 V_{DD}	V V
V_{IH}	High-level input voltage	V_{DD} = 4.5 – 5.5 V V_{DD} = 3.0 – 3.6 V	2.0 0.7 V_{DD}	– –	– –	V V
V_{OL}	Low-level output voltage	V_{DD} = 4.5 – 5.5 V, I_{OL}= 16 mA V_{DD} = 3.0 – 3.6 V, I_{OL}= 8 mA	– –	– –	0.4 0.4	V V
V_{OHCMOS}	High-level output voltage, CMOS levels	V_{DD} = 4.5 – 5.5 V, I_{OH}= –16 mA V_{DD} = 3.0 – 3.6 V, I_{OH}= –8 mA	V_{DD} – 0.4 V_{DD} – 0.4	– –	– –	V V
V_{OHTTL}	High-level output voltage, TTL levels	V_{DD} = 4.5 – 5.5 V, I_{OH}= –8 mA	2.4	–	–	V
I_{IL}	Input low current	V_{IN} = 0 V	–	–	10	µA
I_{IH}	Input high current	V_{IN} = V_{DD}	–	–	5	µA
I_{DD}	Power supply current, Unloaded	V_{DD} = 4.5 – 5.5 V, output frequency <= 133 MHz V_{DD} = 3.0 – 3.6 V, output frequency <= 100 MHz	– –	– –	45 25	mA mA
I_{DDS}[3]	Stand-by current (PD = 0)	V_{DD} = 4.5 – 5.5 V V_{DD} = 3.0 – 3.6 V	– –	25 10	100 50	µA
R_{UP}	Input pull up resistor	V_{DD} = 4.5 – 5.5 V, V_{IN} = 0 V V_{DD} = 4.5 – 5.5 V, V_{IN} = 0.7 V_{DD}	1.1 50	3.0 100	8.0 200	MΩ kΩ
I_{OE_CLKOUT}	CLKOUT pull down current	V_{DD} = 5.0	–	20	–	µA

Output Clock Switching Characteristics Industrial

Over the Operating Range[4]

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
t_{1w}	Output duty cycle at 1.4 V, V_{DD} = 4.5 – 5.5 V $t_{1w} = t_{1A} \div t_{1B}$	1 – 40 MHz, C_L <= 35 pF 40 – 125 MHz, C_L <= 15 pF 125 – 133 MHz, C_L <= 10 pF	45 45 45		55 55 55	% % %
t_{1x}	Output duty cycle at V_{DD}/2, V_{DD} = 4.5 – 5.5 V $t_{1x} = t_{1A} \div t_{1B}$	1 – 40 MHz, C_L <= 35 pF 40 – 125 MHz, C_L <= 15 pF 125 – 133 MHz, C_L <= 10 pF	45 45 45		55 55 55	% % %
t_{1y}	Output duty cycle at V_{DD}/2, V_{DD} = 3.0 – 3.6 V $t_{1y} = t_{1A} \div t_{1B}$	1– 40 MHz, C_L <= 20 pF 40 – 100 MHz, C_L <= 10 pF	45 40		55 60	% %
t_2	Output clock rise time	Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 35 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 15 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 10 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 4.5 V – 5.5 V, C_L = 35 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 20 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 10 pF	– – – – – –		1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_3	Output clock fall time	Between 0.8 V – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 35 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 15 pF Between 0.8 – 2.0 V, V_{DD} = 4.5 V – 5.5 V, C_L = 10 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 4.5 V – 5.5 V, C_L = 35 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 20 pF Between 0.2 V_{DD} – 0.8 V_{DD}, V_{DD}= 3.0 V – 3.6 V, C_L = 10 pF	– – – – – –		1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_4	Startup time out of Power down	PWR_DWN pin LOW to HIGH[5]	–	1	2	ms
t_{5a}	Power down delay time (synchronous setting)	PWR_DWN pin LOW to output LOW (T= period of output clk)	–	T/2	T+10	ns
t_{5b}	Power down delay time (asynchronous setting)	PWR_DWN pin LOW to output LOW	–	10	15	ns
t_6	Power up time	From power on[5]	–	1	2	ms
t_{7a}	Output Disable time (synchronous setting)	OE pin LOW to output high-Z (T= period of output clk)	–	T/2	T + 10	ns
t_{7b}	Output Disable time (asynchronous setting)	OE pin LOW to output high-Z	–	10	15	ns
t_8	Output Enable time (always synchronous enable)	OE pin LOW to HIGH (T = period of output clk)	–	T	1.5T + 25ns	ns
t_9	Peak-to-peak period jitter	V_{DD} = 3.0 V – 3.6 V, 4.5 V – 5.5 V, Fo > 33 MHz, V_{CO} > 100 MHz V_{DD} = 3.0 V – 5.5 V, Fo < 33 MHz	– –	80 0.3%	150 1%	ps % of F_O

Switching Waveforms

Figure 2. Duty Cycle Timing (t_{1w}, t_{1x}, t_{1y})

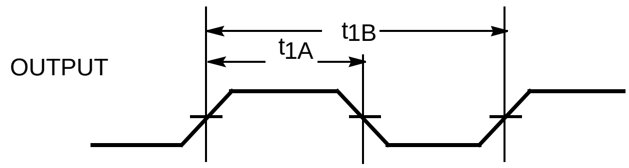


Figure 3. Output Rise/Fall Time

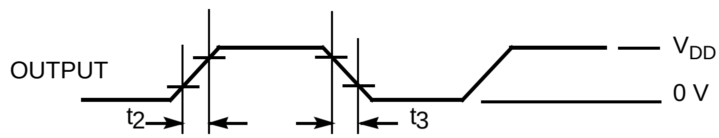


Figure 4. Power down Timing (synchronous and asynchronous modes)

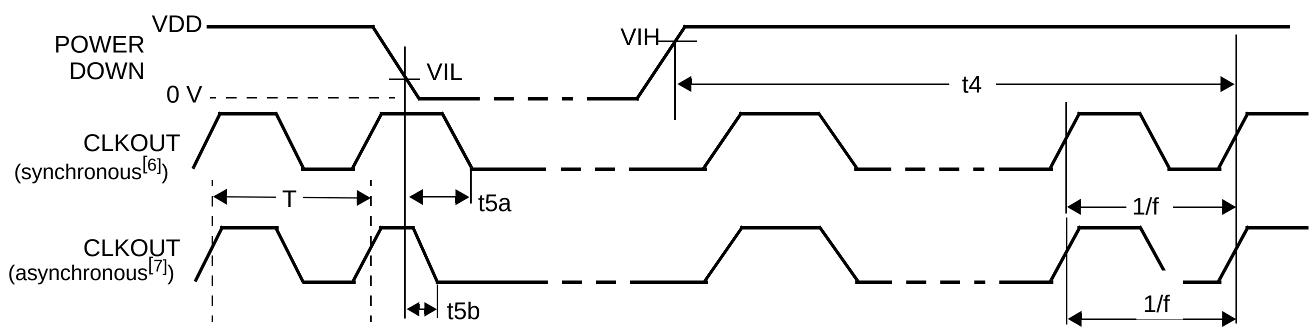


Figure 5. Power up Timing

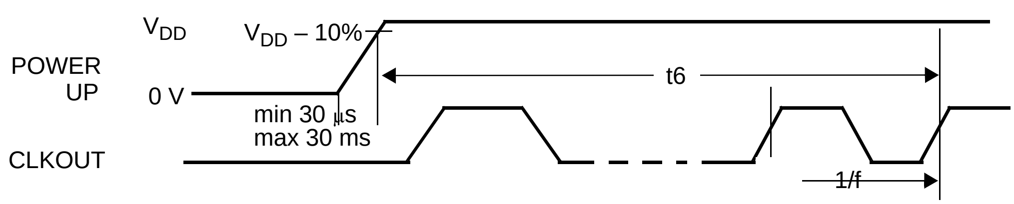
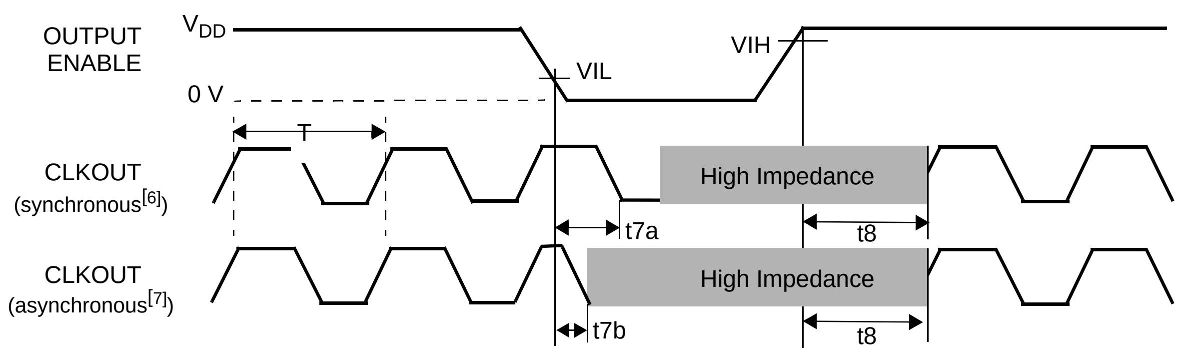


Figure 6. Output Enable Timing (synchronous and asynchronous modes)



Notes
6. In synchronous mode, the power down or output three-state is not initiated until the next falling edge of the output clock.
7. In asynchronous mode, the power down or output three-state occurs within 25 ns regardless of position in the output clock cycle.

Typical Rise/Fall Time[8] Trends for CY2077

Figure 7. Rise/Fall Time vs. VDD over Temperatures

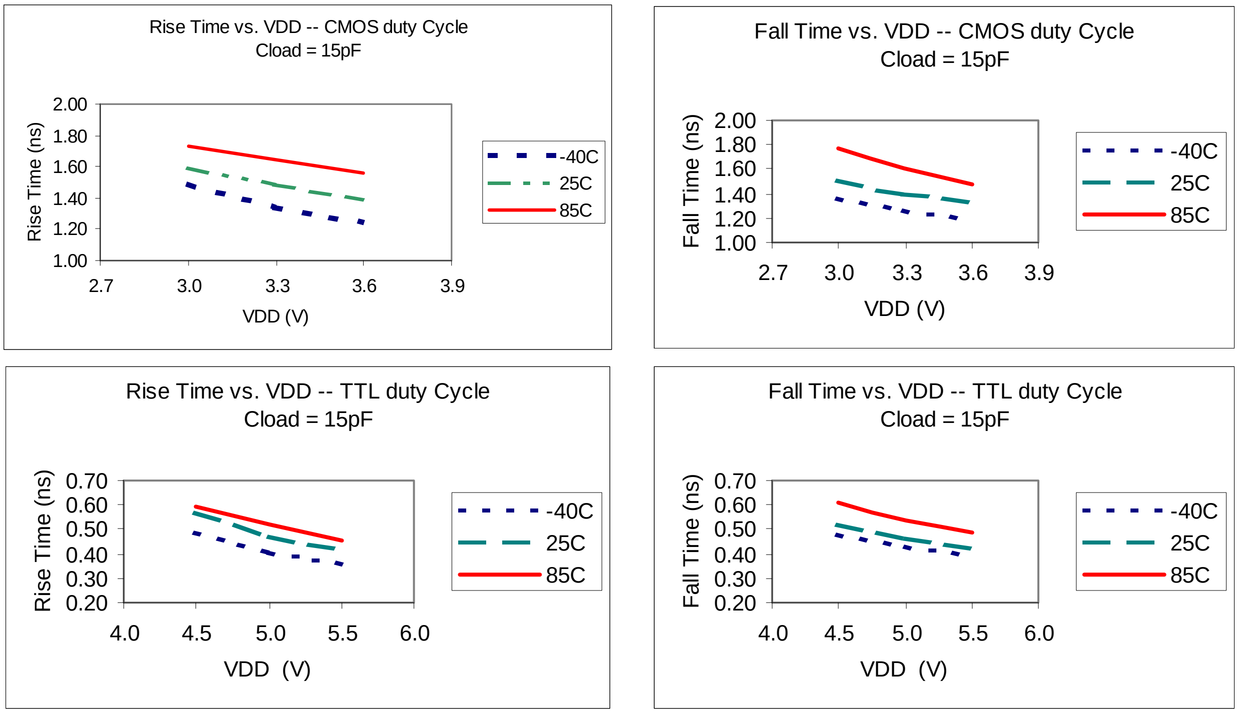
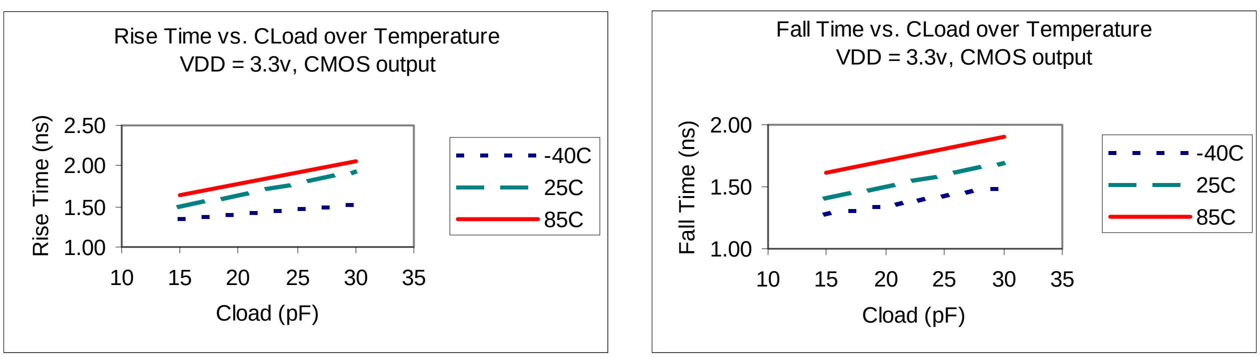


Figure 8. Rise/Fall Time vs. Output Loads over Temperatures



Note

8. Rise/Fall time for CMOS output is measured between 1.2 V_{DD} and 0.8 V_{DD}. Rise/Fall time for TTL output is measured between 0.8 V and 2.0 V.

Typical Duty Cycle[9] Trends for CY2077

Figure 9. Duty Cycle vs. V_{DD} over Temperatures

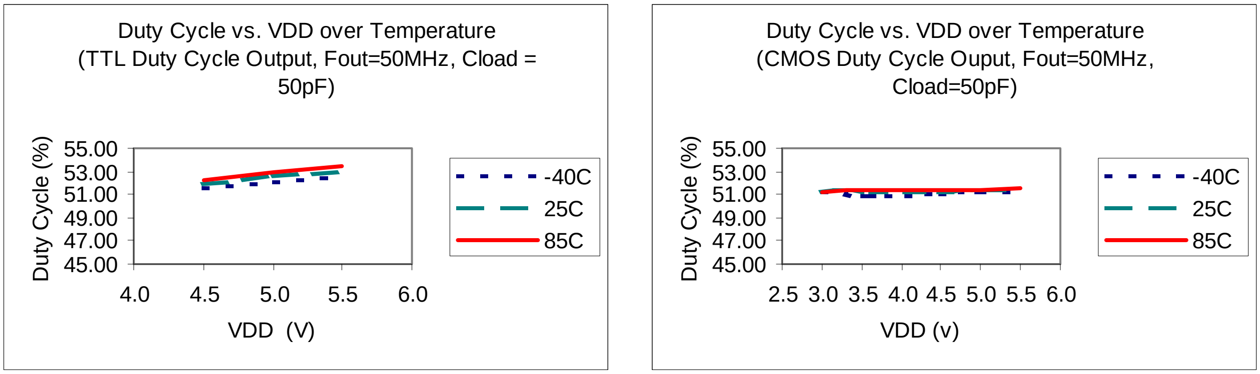


Figure 10. Duty Cycle vs. Output Load

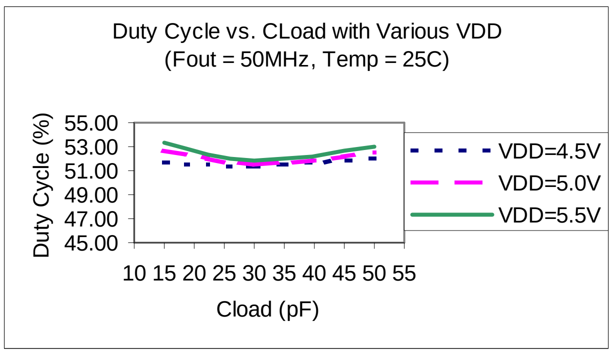
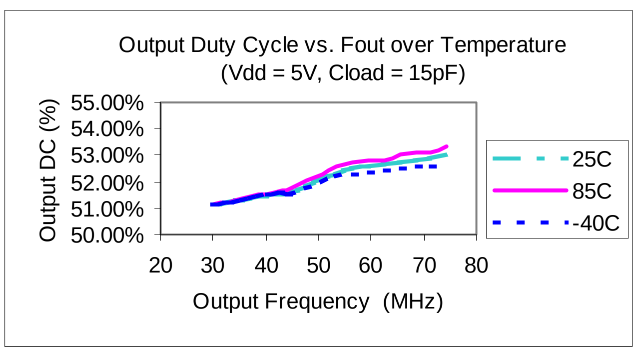


Figure 11. Duty Cycle vs. Output Frequency over Temperatures



Note

9. Duty cycle is measured at 1.4 V for TTL output and 0.5 V_{DD} for CMOS output.

Typical Jitter Trends for CY2077

Figure 12. Period Jitter (pk-pk) vs. V_{DD} over Temperatures

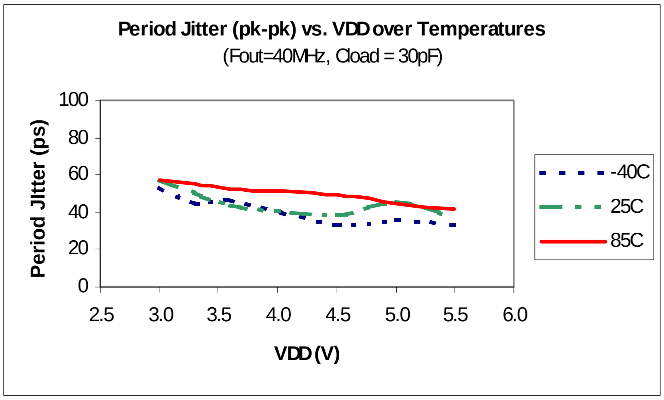
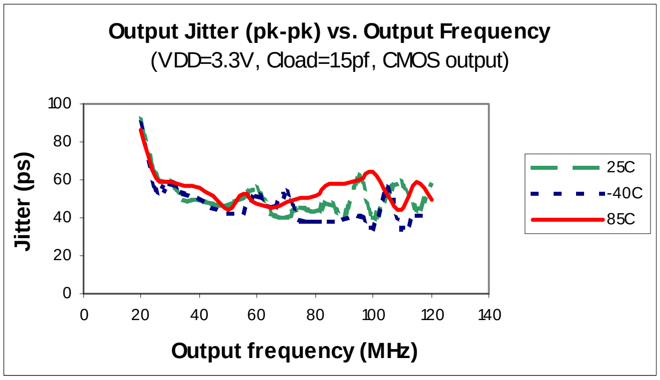
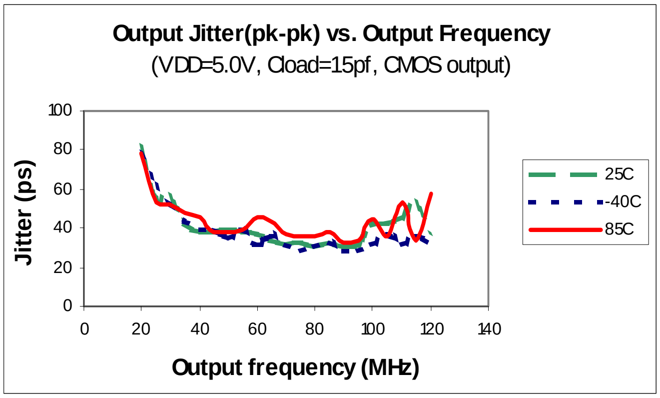


Figure 13. Period Jitter (pk-pk) vs. Output Frequency over Temperatures





Programming Procedures

Currently the CY2077 is available only as a field-programmable device, as indicated by an “F” in the ordering code.

Devices may be programmed using the CY3672-USB programmer, or through programmers available from third party programmer manufacturers such as Hi-Lo Systems and BP Micro. Programming services are also available from third parties, including some Cypress distribution partners.

To generate a JEDEC format programming file, customers must use CyClocks software. This software automatically calculates the output frequencies that can be generated by CY2077 devices. The CyClocks software is a subset of the larger software tool CyberClocks, which is available free of charge from the Cypress web site (http://www.cypress.com). CyberClocks is installed on a PC and must not be confused with the web-based application CyberClocks Online.

For high volume designs, factory programming of customer-specific configurations is available on other 8-pin devices such as the CY22180, CY22801 and CY22381. Factory programming is no longer offered for new designs using the CY2077.

Ordering Information

Order Code[11]	Package Name	Package Type	Operating Temp. Range	Operating Voltage
Pb-Free				
CY2077FSXC	S8	8-pin SOIC	Commercial (T = 0 °C to 70 °C)	3.3 V or 5 V
CY2077FSXCT	S8	8-pin SOIC–Tape and Reel	Commercial (T = 0 °C to 70 °C)	3.3 V or 5 V
CY2077FZZ	Z8	8-pin TSSOP	Commercial (T = 0 °C to 70 °C)	3.3 V or 5 V
CY2077FZXI	Z8	8-pin TSSOP	Industrial (T = –40 °C to 85 °C)	3.3 V or 5 V
CY2077FZXIT	Z8	8-pin TSSOP–Tape and Reel	Industrial (T = –40 °C to 85 °C)	3.3 V or 5 V
Programmer				
CY3672-USB	Programming Kit			
CY3696	Socket adapter board, for programming CY2077FS (SOIC Package)			
CY3697	Socket adapter board, for programming CY2077FZ (TSSOP Package)			

Table 4. Obsolete or Not For New Designs

Original Device		Replacement Device	
Order Code[10, 11]	**Description**	**Order Code**	**Description**
CY2077SC-xxx		none	
CY2077SC-xxxT		none	
CY2077SI-xxx		none	
CY2077SI-xxxT		none	
CY2077SXC-xxx		none	
CY2077SXC-xxxT		none	
CY2077ZC-xxx		none	
CY2077ZC-xxxT		none	
CY2077ZI-xxx		none	
CY2077ZI-xxxT		none	
CY2077ZXC-xxx		none	
CY2077ZXC-xxxT		none	
CY2077FSI	SOIC, Industrial (T = –40 °C to 85 °C)	CY2077FSXC	Pb-free SOIC, Commercial
CY2077FZ	TSSOP, Commercial (T = 0 °C to 70 °C)	CY2077FZZ	Pb-free TSSOP, Commercial
CY2077FZI	TSSOP, Industrial (T = –40 °C to 85 °C)	CY2077FZXI	Pb-free TSSOP, Industrial

Notes

10. The CY2077SC-xxx(T), CY2077SI-xxx(T), CY2077SXC-xxx(T), CY2077ZC-xxx(T), CY2077ZI-xxx(T) andCY2077ZXC-xxx(T), are factory programmed configurations. Factory programming is available for high-volume design opportunities. For more details, contact your local Cypress FAE or Cypress Sales Representative.
11. The CY2077F are field programmable. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Package Diagrams

Figure 14. 8-pin (150 mil Body) SOIC (Small Outline IC)

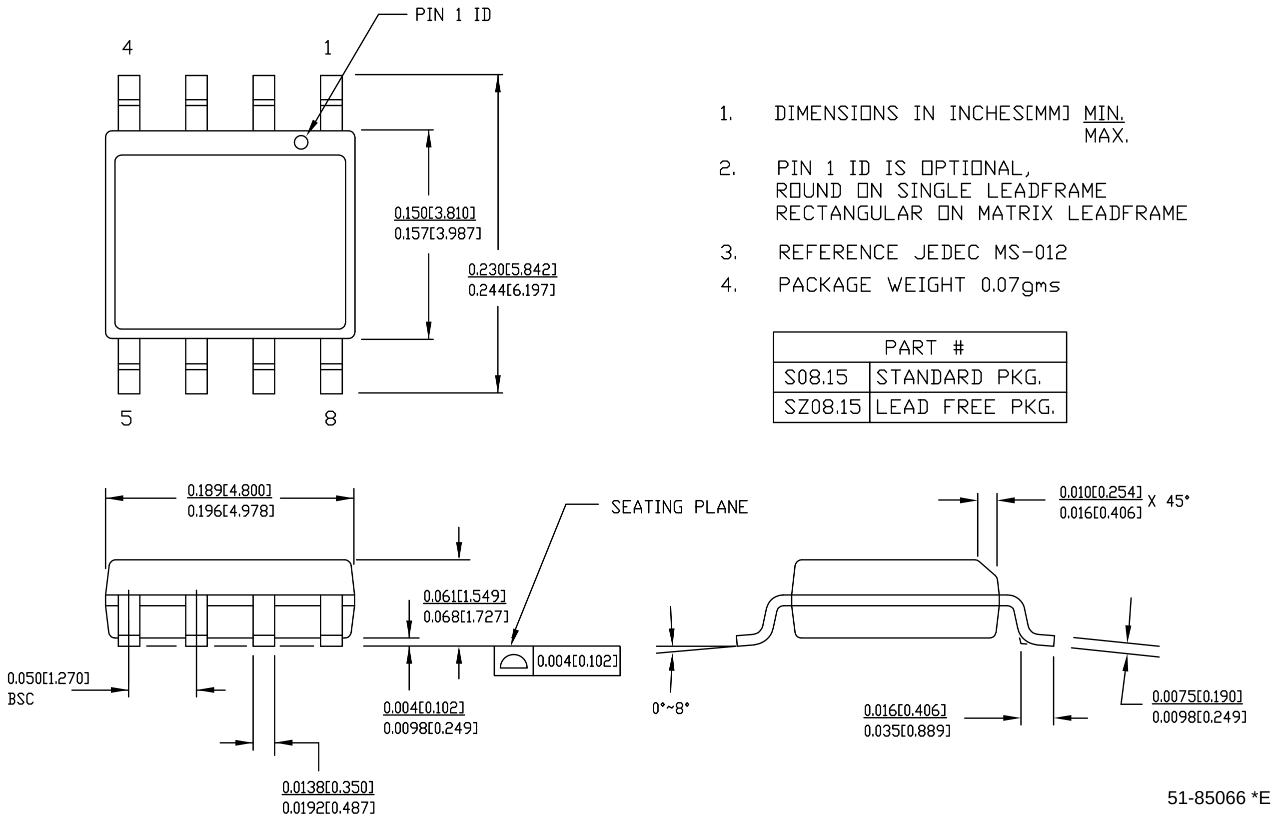
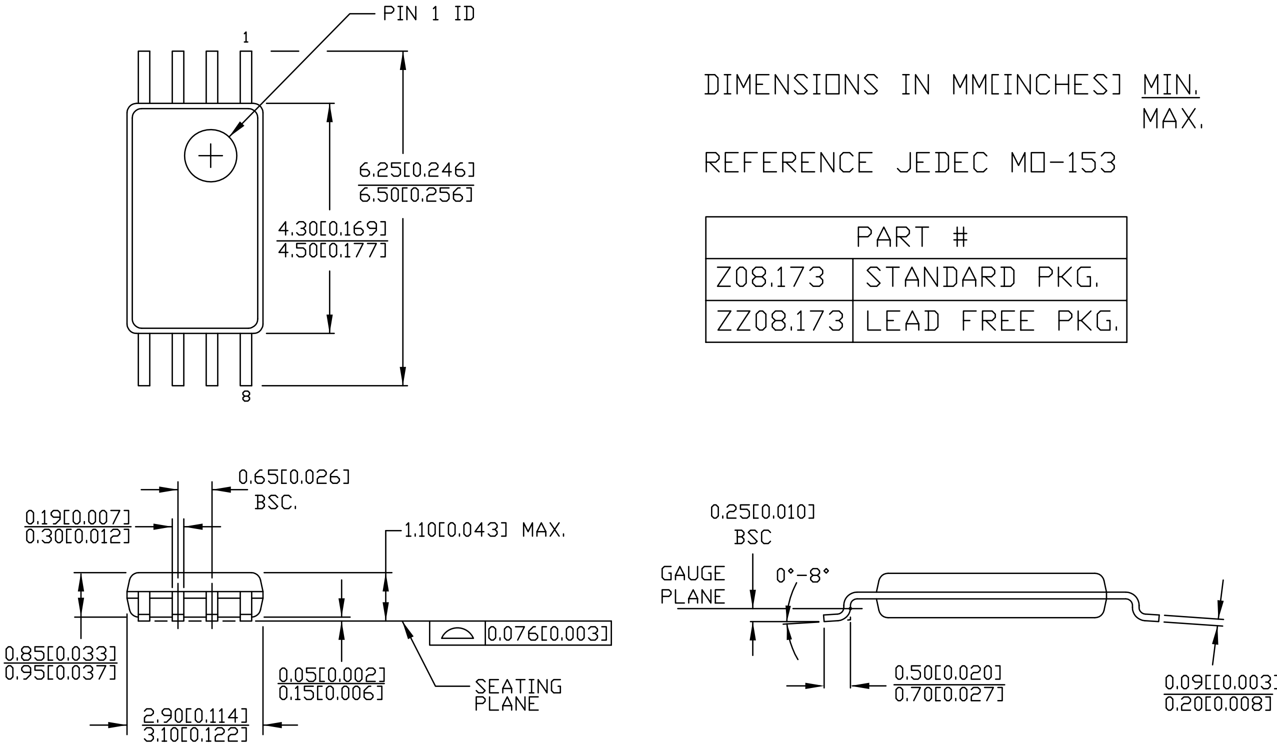


Figure 15. 8-pin (4.40-mm Body) TSSOP (Thin Shrunk Small Outline Package)



51-85093 *D

Document History Page

Document Title: CY2077 High-accuracy EPROM Programmable Single-PLL Clock Generator Document Number: 38-07210				
Revision	**ECN**	**Orig. of Change**	**Sumbission Date**	**Description of Change**
**	111727	DSG	02/07/02	Convert from Spec number: 38-01009 to 38-07210
*A	114938	CKN	07/24/02	Added table and notes to page 11
*B	121843	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*C	2104546	PYG/KVM /AESA	See ECN	Updated Ordering Information table Replaced the “Custom Configuration Request Procedure” section with “Programming Procedures” Updated package diagrams
*D	2631183	KVM/AESA	01/06/09	Updated template. CY2077FS removed from the active part number table. Added CY2077FZXI and CY2077FZXIT to the Ordering Information table. Corrected wording on p. 2 about when the weak output pull-down is active. Added to Table 1 to indicate that PWR_DWN is active low and OE is active high.
*E	2905892	CXQ	04/07/10	Removed inactive part CY2077FS from Table 4. Updated package diagrams.
*F	3388539	MNSB/ PURU	09/29/11	Replaced “CY3670” with “CY3672-USB” under Programming Procedures on page 13. Updated Ordering Information on page 13 to include correct programmer part numbers and socket adapters.
*G	3514611	PURU	02/01/2012	Removed benefits section Updated Package Diagrams

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