74AHC259; 74AHCT259

8-bit addressable latch

Rev. 02 — 15 May 2008 Product data sheet

1. General description

The 74AHC259; 74AHCT259 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC259; 74AHCT259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single-line data in eight addressable latches and providing a 3-to-8 decoder and multiplexer function with active HIGH outputs (Q0 to Q7). It also incorporates an active LOW common reset ($\overline{MR}$) for resetting all latches as well as an active LOW enable input ($\overline{LE}$).

The 74AHC259; 74AHCT259 has four modes of operation:

- In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states.
- In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.
- In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the data input (D) with all other outputs in the LOW state.
- In the reset mode, all outputs are LOW and unaffected by the address inputs (A0 to A2) and data input (D).

When operating the 74AHC259; 74AHCT259 as an address latch, changing more than one bit of the address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Inputs accept voltages higher than V_{CC}

- Input levels:
  - For 74AHC259: CMOS level
  - For 74AHCT259: TTL level
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC259				
74AHC259D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC259PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT259				
74AHCT259D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT259PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

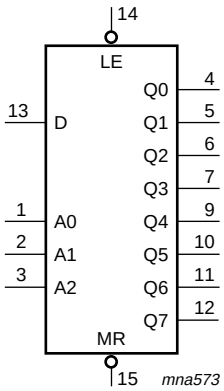


Fig 1. Logic symbol

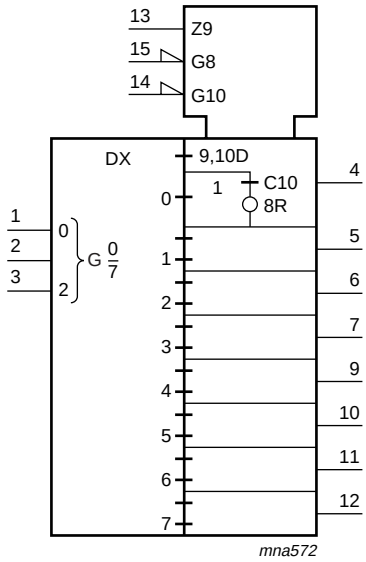


Fig 2. IEC logic symbol

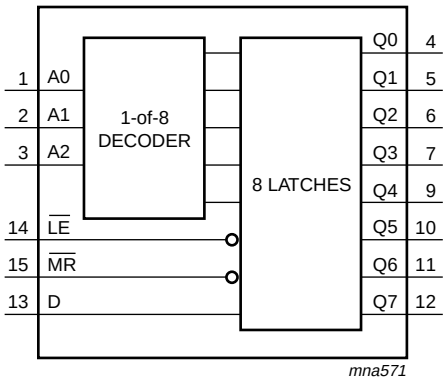


Fig 3. Functional diagram

5. Pinning information

5.1 Pinning

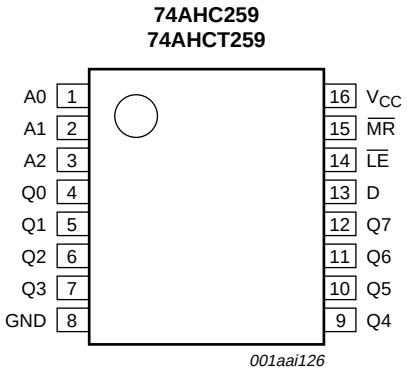


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input
A1	2	address input
A2	3	address input
Q0	4	latch output
Q1	5	latch output
Q2	6	latch output
Q3	7	latch output
GND	8	ground (0 V)
Q4	9	latch output
Q5	10	latch output

Table 2. Pin description *...continued*

Symbol	Pin	Description
Q6	11	latch output
Q7	12	latch output
D	13	data input
$\overline{LE}$	14	latch enable input (active LOW)
$\overline{MR}$	15	conditional reset input (active LOW)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Input						Output							
	$\overline{MR}$	$\overline{LE}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset (clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel) decoder (when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
			d	H	L	L	L	Q = d	L	L	L	L	L	L
			d	L	H	L	L	L	Q = d	L	L	L	L	L
			d	H	H	L	L	L	L	Q = d	L	L	L	L
			d	L	L	H	L	L	L	L	Q = d	L	L	L
			d	H	L	H	L	L	L	L	L	Q = d	L	L
			d	L	H	H	L	L	L	L	L	L	Q = d	L
			d	H	H	H	L	L	L	L	L	L	L	Q = d
Memory (no action)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
			d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
			d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
			d	H	H	L	q_0	q_1	q_2	Q = d	q_4	q_5	q_6	q_7
			d	L	L	H	q_0	q_1	q_2	q_3	Q = d	q_5	q_6	q_7
			d	H	L	H	q_0	q_1	q_2	q_3	q_4	Q = d	q_6	q_7
			d	L	H	H	q_0	q_1	q_2	q_3	q_4	q_5	Q = d	q_7
			H	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition;
q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

Table 4. Operating mode select table[1]

$\overline{LE}$	$\overline{MR}$	Mode
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V	[1]	–20	-	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	–20	+20	mA
I_O	output current	$V_O = –0.5$ V to ($V_{CC} + 0.5$ V)		–25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			–75	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = –40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC259						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0$ V to 3.6 V	-	-	100	ns/V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	20	ns/V
74AHCT259						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5$ V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC259										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = –50 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF
74AHCT259										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other pins at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC259										
t_{pd}	propagation delay	D to Qn; see Figure 5 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.8	11.5	1.0	13.5	1.0	15.0	ns
		C_L = 50 pF	-	7.3	14.5	1.0	17.0	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.1	7.5	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF	-	5.3	9.5	1.0	11.0	1.0	12.0	ns
		An to Qn; see Figure 6 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	7.5	14.5	1.0	17.0	1.0	18.5	ns
		C_L = 50 pF	-	9.1	18.0	1.0	21.0	1.0	23.0	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	5.3	9.5	1.0	11.5	1.0	12.5	ns
		C_L = 50 pF	-	6.5	11.5	1.0	13.5	1.0	15.0	ns
		$\overline{LE}$ to Qn; see Figure 7 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	6.2	12.0	1.0	14.0	1.0	15.2	ns
		C_L = 50 pF	-	7.7	15.5	1.0	17.5	1.0	19.0	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.3	8.0	1.0	9.5	1.0	10.5	ns
		C_L = 50 pF	-	5.5	10.0	1.0	11.5	1.0	12.5	ns

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	$\overline{MR}$ to Qn; see Figure 8 [3]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.4	10.5	1.0	12.5	1.0	13.5	ns
		C_L = 50 pF	-	7.0	13.5	1.0	15.5	1.0	17.0	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.9	7.0	1.0	8.5	1.0	9.5	ns
		C_L = 50 pF	-	5.1	9.0	1.0	10.5	1.0	11.5	ns
t_W	pulse width	$\overline{LE}$ HIGH or LOW; see Figure 7								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{MR}$ LOW; see Figure 8								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	D, An to $\overline{LE}$; see Figure 9 and Figure 10								
		V_{CC} = 3.0 V to 3.6 V	4.0	-	-	4.0	-	4.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	4.0	-	-	4.0	-	4.0	-	ns
t_h	hold time	D, An to $\overline{LE}$; see Figure 9 and Figure 10								
		V_{CC} = 3.0 V to 3.6 V	1.0	-	-	1.0	-	1.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	1.0	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	13	-	-	-	-	-	pF
74AHCT259; V_{CC} = 4.5 V to 5.5 V										
t_{pd}	propagation delay	D to Qn; see Figure 5 [2]								
		C_L = 15 pF	-	4.1	7.5	1.0	9.0	1.0	10.0	ns
		C_L = 50 pF	-	5.4	9.5	1.0	11.0	1.0	12.0	ns
		An to Qn; see Figure 6 [2]								
		C_L = 15 pF	-	5.5	9.5	1.0	11.5	1.0	12.5	ns
		C_L = 50 pF	-	6.6	12.0	1.0	14.0	1.0	15.5	ns
		$\overline{LE}$ to Qn; see Figure 7 [2]								
		C_L = 15 pF	-	4.3	8.0	1.0	9.5	1.0	10.4	ns
		C_L = 50 pF	-	5.5	10.0	1.0	12.0	1.0	13.0	ns
		$\overline{MR}$ to Qn; see Figure 8 [3]								
		C_L = 15 pF	-	3.9	7.0	1.0	8.5	1.0	9.5	ns
		C_L = 50 pF	-	5.1	9.0	1.0	10.5	1.0	11.5	ns
t_W	pulse width	$\overline{LE}$ HIGH or LOW; see Figure 7	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{MR}$ LOW; see Figure 8	5.0	-	-	5.0	-	5.0	-	ns

Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{su}	set-up time	D, An to $\overline{LE}$; see Figure 9 and Figure 10	4.0	-	-	4.0	-	4.0	-	ns
t_h	hold time	D, An to $\overline{LE}$; see Figure 9 and Figure 10	1.0	-	-	1.0	-	1.0	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	17	-	-	-	-	-	pF

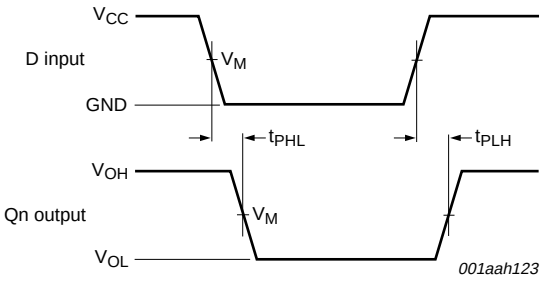
[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{pd} is the same as t_{PHL} only.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

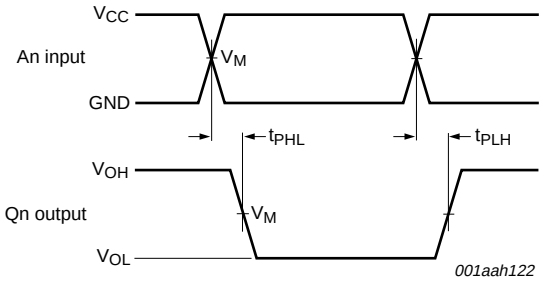
11. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

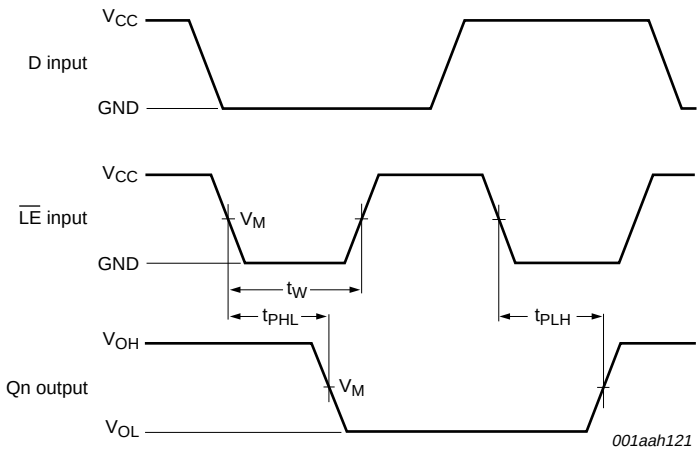
Fig 5. Data input to output propagation delays



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

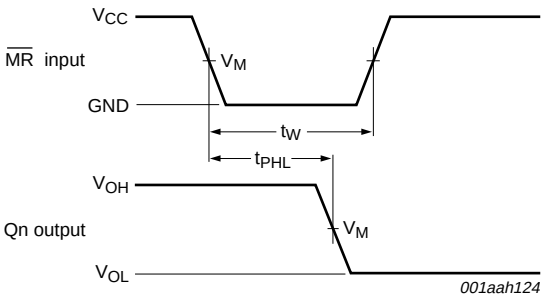
Fig 6. Address input to output propagation delays



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

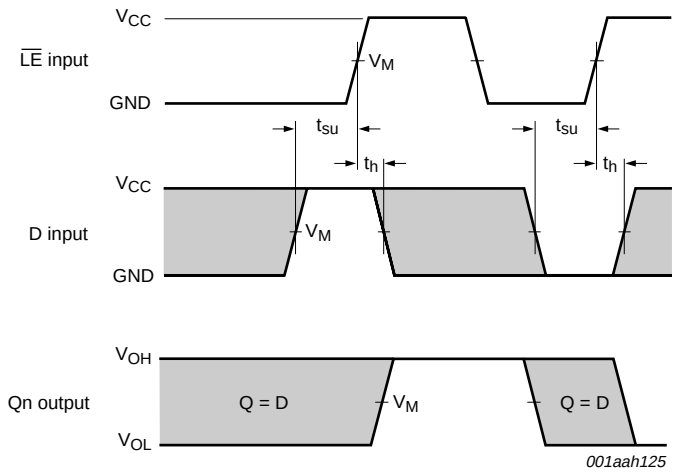
Fig 7. Enable input to output propagation delays and pulse width



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Conditional reset input to output propagation delays

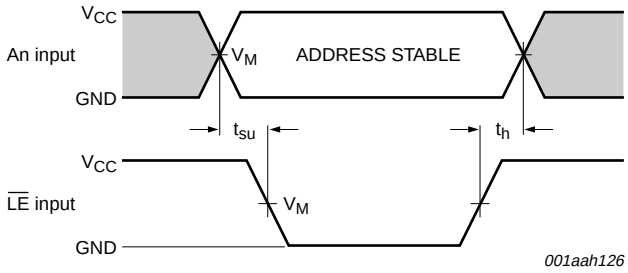


Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data input to latch enable input set-up and hold times



Measurement points are given in Table 9.

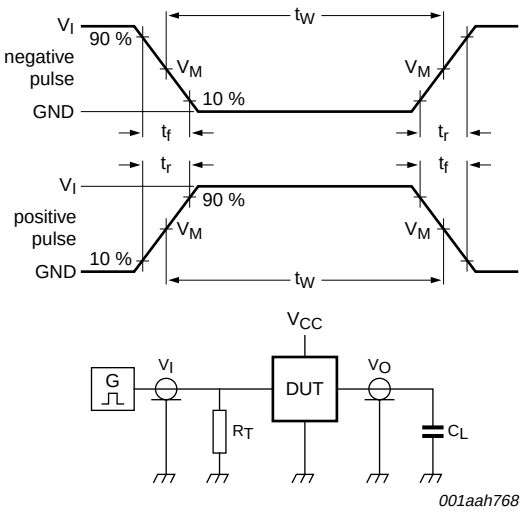
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. Address input to latch enable input set-up and hold times

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74AHC259	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT259	1.5 V	$0.5 \times V_{CC}$



Test data is given in Table 10.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

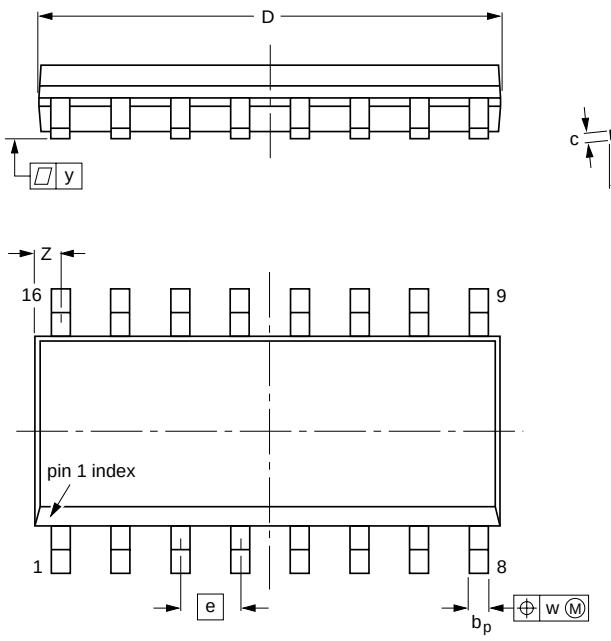
Fig 11. Load circuitry for measuring switching times

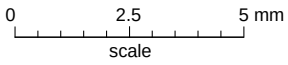
Table 10. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC259	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT259	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

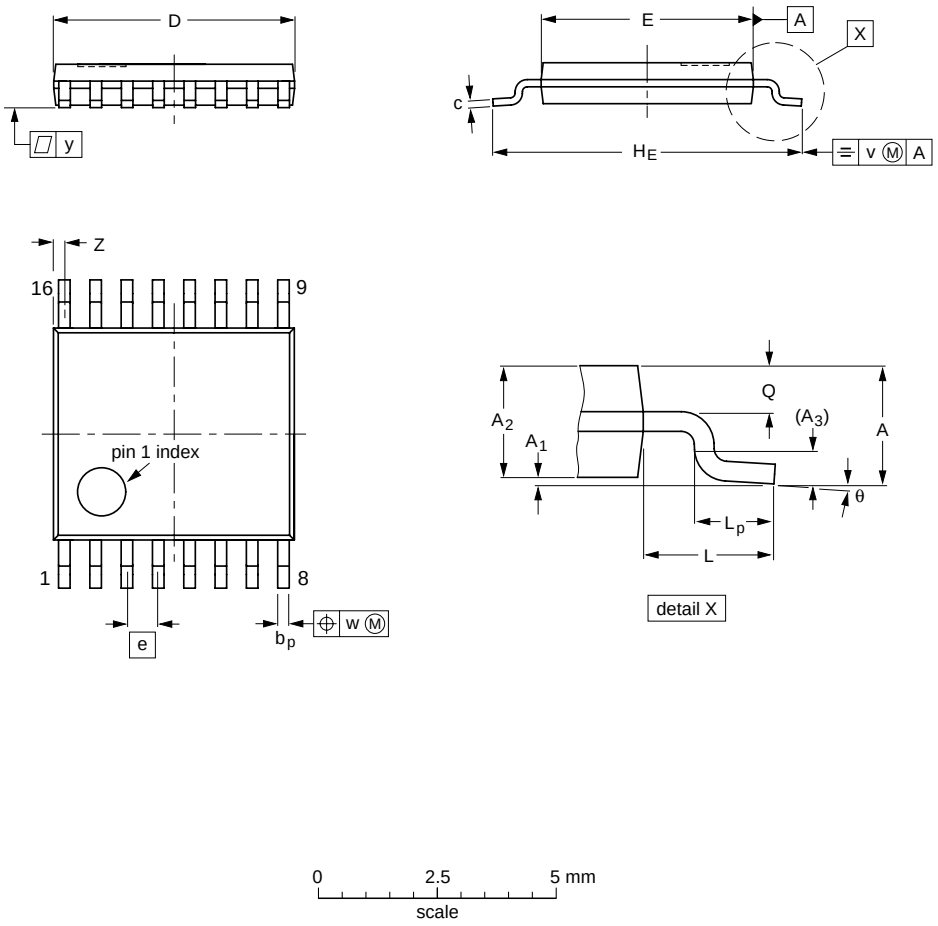
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT259_2	20080515	Product data sheet	-	74AHC_AHCT259_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6: the conditions for input leakage current have been changed.			
74AHC_AHCT259_1	20000314	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 15 May 2008

Document identifier: 74AHC_AHCT259_2

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