

- **Excellent Output Drive Capability**
 $V_O = \pm 2.5 \text{ V Min at } R_L = 100 \, \Omega$,
 $V_{CC\pm} = \pm 5 \text{ V}$
 $V_O = \pm 12.5 \text{ V Min at } R_L = 600 \, \Omega$,
 $V_{CC\pm} = \pm 15 \text{ V}$
- **Low Supply Current . . . 280 μA Typ**
- **Decompensated for High Slew Rate and Gain-Bandwidth Product**
 $A_{VD} = 0.5 \text{ Min}$
Slew Rate = 10 V/μs Typ
Gain-Bandwidth Product = 6.5 MHz Typ

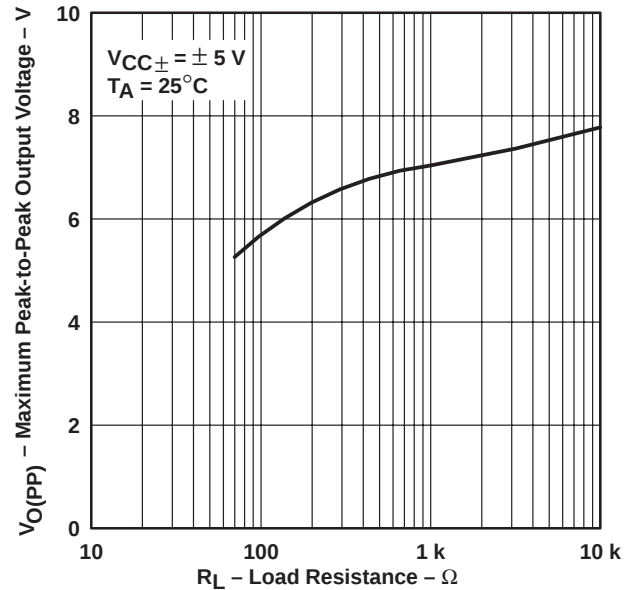
- **Wide Operating Supply Voltage Range**
 $V_{CC\pm} = \pm 3.5 \text{ V to } \pm 18 \text{ V}$
- **High Open-Loop Gain . . . 280 V/mV Typ**
- **Low Offset Voltage . . . 500 μV Max**
- **Low Offset Voltage Drift With Time**
0.04 μV/Month Typ
- **Low Input Bias Current . . . 5 pA Typ**

description

The TLE2161, TLE2161A, and TLE2161B are JFET-input, low-power, precision operational amplifiers manufactured using the Texas Instruments Excalibur process. Decompensated for stability with a minimum closed-loop gain of 5, these devices combine outstanding output drive capability with low power consumption, excellent dc precision, and high gain-bandwidth product.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a device that remains precise even with changes in temperature and over years of use.

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE**



AVAILABLE OPTIONS

T_A	V_{IOmax} AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV 1.5 mV 3 mV	— TLE2161ACD TLE2161CD	— —	— —	TLE2161BCP TLE2161ACP TLE2161CP
–40°C to 85°C	500 μV 1.5 mV 3 mV	— TLE2161AID TLE2161ID	— —	— —	TLE2161BIP TLE2161AIP TLE2161IP
–55°C to 125°C	500 μV 1.5 mV 3 mV	— TLE2161AMD TLE2161MD	— TLE2161AMFK TLE2161MFK	TLE2161BMJG TLE2161AMJG TLE2161MJG	TLE2161BMP TLE2161AMP TLE2161MP

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2161ACDR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
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TLE2161, TLE2161A, TLE2161B

EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE

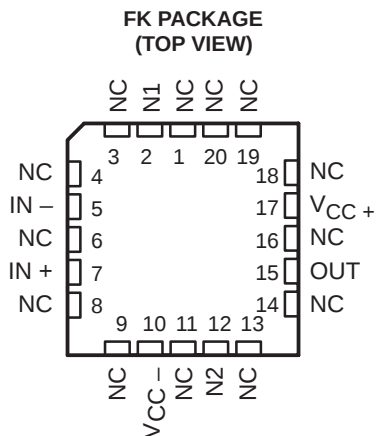
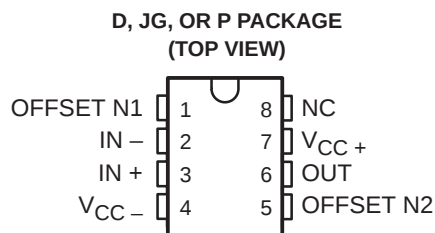
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description (continued)

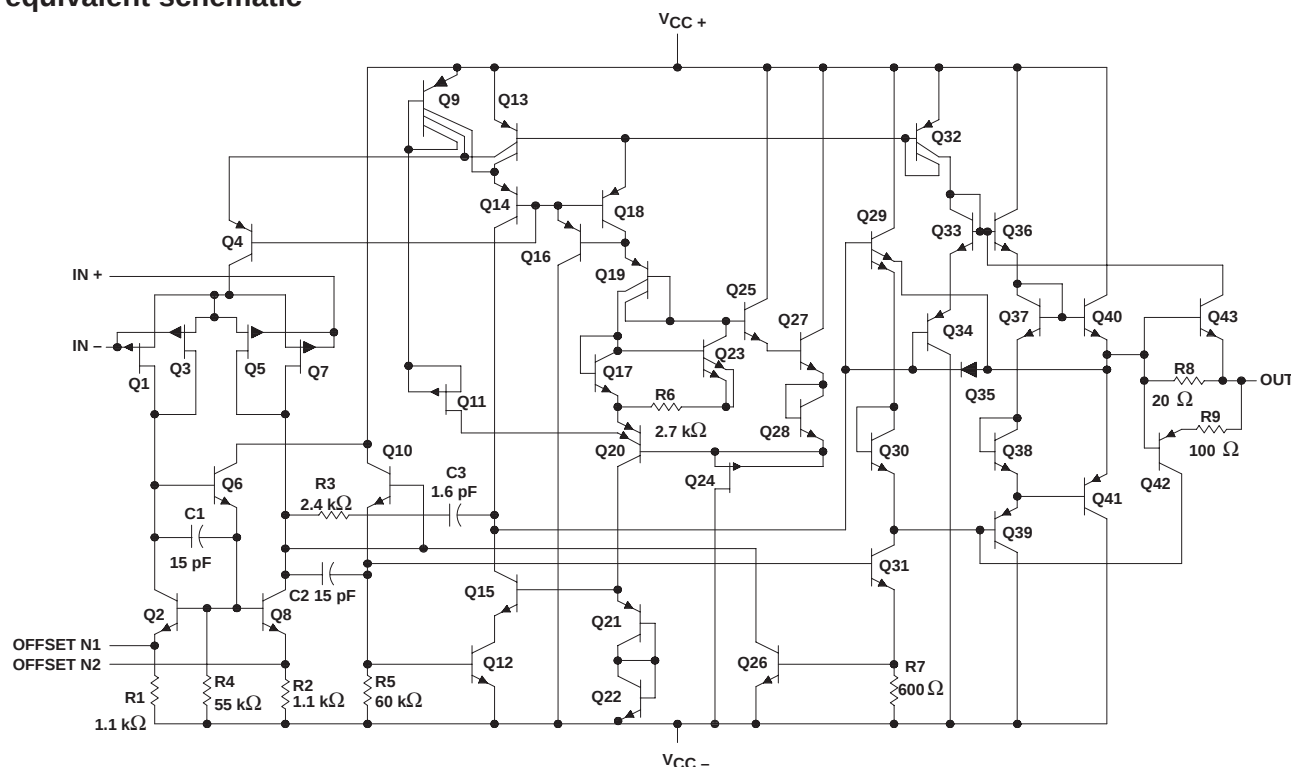
A variety of available options includes small-outline packages and chip-carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.



NC – No internal connection

equivalent schematic



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC+} (see Note 1)	19 V
Supply voltage, V_{CC-}	– 19 V
Differential input voltage, V_{ID} (see Note 2)	± 38 V
Input voltage range, V_I (any input)	V_{CC+} to V_{CC-}
Input current, I_I (each input)	± 1 mA
Output current, I_O	± 80 mA
Total current into V_{CC+}	80 mA
Total current out of V_{CC-}	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	– 40°C to 85°C
M suffix	– 55°C to 125°C
Storage temperature range, T_{stg}	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60seconds: JG package	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
2. Differential voltages are at $IN+$ with respect to $IN-$.
3. The output may be shorted to either supply. Temperature and /or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	+3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC+} \pm 5\text{ V}$	–1.6	4	–1.6	4	–1.6	4	V
	$V_{CC+} \pm 15\text{ V}$	–11	13	–11	13	–11	13	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

TLE2161, TLE2161A, TLE2161B

EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE

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electrical characteristics at specified free-air temperature, $V_{CC} \pm \pm 5 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2161C, TLE2161AC TLE2161BC			UNIT
				MIN	TYP	MAX	
V _{IO} Input offset voltage	TLE2161C	V _{IC} = 0, R _S = 50 Ω	25°C	0.8		3.1	mV
	TLE2161AC		Full range	4			
			25°C	0.6		2.6	
			Full range	3.5			
			25°C	0.5		1.9	
	TLE2161BC		Full range	2.4			
α _{VIO} Temperature coefficient of input offset voltage			Full range	6		μV/°C	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo	
I _{IO} Input offset current			25°C	1		pA	
I _{IB} Input bias current			Full range	0.8		nA	
			25°C	3		pA	
V _{ICR} Common-mode input voltage range			Full range	2		nA	
		25°C	–1.6 to 4	–2 to 6	V		
V _{OM} + Maximum positive peak output voltage swing	R _L = 10 kΩ	Full range	–1.6 to 4			V	
		25°C	3.5	3.7	V		
	R _L = 100 Ω	Full range	3.3				
		25°C	2.5	3.1			
V _{OM} – Maximum negative peak output voltage swing	R _L = 10 kΩ	Full range	2			V	
		25°C	–3.7	–3.9			
	R _L = 100 Ω	Full range	–3.3				
		25°C	–2.5	–2.7			
A _{VD} Large-signal differential voltage amplification	V _O = ±2.8 V, R _L = 10 kΩ	Full range	–2			V/mV	
		25°C	15	80			
	V _O = 0 to 2 V, R _L = 100 Ω	Full range	2				
		25°C	0.75	45			
	V _O = 0 to –2 V, R _L = 100 Ω	Full range	0.5				
		25°C	0.5	3			
r _i Input resistance		Full range	0.25				
c _i Input capacitance		25°C	10 ¹²		Ω		
z _O Open-loop output impedance	I _O = 0	25°C	4		pF		
CMRR Common-mode rejection ratio	V _{IC} =V _{ICRmin} , R _S = 50 Ω	25°C	280		Ω		
		Full range	65		82	dB	
k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±5 V to ±15 V, R _S = 50 Ω	Full range	65		dB		
		25°C	75	93			
I _{CC} Supply current	V _O = 0, No load	Full range	75		μA		
ΔI _{CC} Supply-current change over operating temperature range		25°C	280			325	
		Full range	350				
		Full range	29		μA		

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{CC} \pm = \pm 5 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLE2161C, TLE2161AC TLE2161BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C	7	10		V/ μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20 \Omega$, $f = 10 \text{ Hz}$	25°C		59	100	nV/ $\sqrt{\text{Hz}}$
		$R_S = 20 \Omega$, $f = 1 \text{ kHz}$			43	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$	25°C		1.1		μV
I_n	Equivalent input noise current	$f = 1 \text{ kHz}$	25°C		1		fA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{O(PP)} = 2 \text{ V}$, $R_L = 10 \text{ k}\Omega$, $A_{VD} = 5$, $f = 10 \text{ kHz}$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C		5.8		MHz
		$f = 100 \text{ kHz}$, $R_L = 100 \text{ k}\Omega$, $C_L = 100 \text{ pF}$			4.3		
t_s	Settling time	$\epsilon = 0.1\%$	25°C		5		μs
		$\epsilon = 0.01\%$			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10 \text{ k}\Omega$	25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C		70°		
		$A_{VD} = 5$, $R_L = 100 \Omega$, $C_L = 100 \text{ pF}$			84°		

[†] Full range is 0°C to 70°C.

TLE2161, TLE2161A, TLE2161B

EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE

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electrical characteristics at specified free-air temperature, $V_{CC} \pm \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2161C, TLE2161AC TLE2161BC			UNIT
				MIN	TYP	MAX	
V _{IO} Input offset voltage	TLE2161C	V _{IC} = 0, R _S = 50 Ω	25°C	0.6		3	mV
	TLE2161AC		Full range	3.9			
			25°C	0.5		1.5	
			Full range	2.5			
			25°C	0.3		0.5	
	TLE2161BC		Full range	1			
αV _{IO} Temperature coefficient of input offset voltage	Full range		6		μV/°C		
Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo	
I _{IO} Input offset current			25°C	2		pA	
			Full range	1		nA	
I _{IB} Input bias current		25°C	4		pA		
		Full range	3		nA		
V _{ICR} Common-mode input voltage range		25°C	–11 to 13	–12 to 16	V		
		Full range	–11 to 13		V		
V _{OM} + Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	13.2	13.7	V		
		Full range	13				
	R _L = 600 Ω	25°C	12.5	13.2			
		Full range	12				
V _{OM} – Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	–13.2	–13.7	V		
		Full range	–13				
	R _L = 600 Ω	25°C	–12.5	–13			
		Full range	–12				
A _{VD} Large-signal differential voltage amplification	V _O = ±10 V, R _L = 10 kΩ	25°C	30	230	V/mV		
		Full range	20				
	V _O = 0 to 8 V, R _L = 600 Ω	25°C	25	100			
		Full range	10				
	V _O = 0 to –8 V, R _L = 600 Ω	25°C	3	25			
		Full range	1				
r _i Input resistance		25°C	10 ¹²		Ω		
c _i Input capacitance		25°C	4		pF		
z _o Open-loop output impedance	I _O = 0	25°C	280		Ω		
CMRR Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	72	90	dB		
		Full range	70				
k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±5 V to ±15 V, R _S = 50 Ω	25°C	75	93	dB		
		Full range	75				
I _{CC} Supply current	V _O = 0, No load	25°C	290	350	μA		
		Full range	375				
ΔI _{CC} Supply-current change over operating temperature range			Full range	34		μA	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE
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operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLE2161C, TLE2161AC TLE2161BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	7	10		V/ μ s
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20\text{ }\Omega$, $f = 10\text{ Hz}$	25°C		70	100	nV/ $\sqrt{\text{Hz}}$
		$R_S = 20\text{ }\Omega$, $f = 1\text{ kHz}$			40	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		μ V
I_n	Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1.1		fA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{O(PP)} = 2\text{ V}$, $A_{VD} = 5$, $f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		6.4		MHz
		$f = 100\text{ kHz}$, $R_L = 600\text{ }\Omega$, $C_L = 100\text{ pF}$			5.6		
t_s	Settling time	$\epsilon = 0.1\%$	25°C		5		μ s
		$\epsilon = 0.01\%$			10		
B _{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10\text{ k}\Omega$	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		72°		
		$A_{VD} = 5$, $R_L = 600\text{ }\Omega$, $C_L = 100\text{ pF}$			78°		

[†] Full range is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, $V_{CC} \pm = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2161I, TLE2161AI TLE2161BI			UNIT
				MIN	TYP	MAX	
V _{IO} Input offset voltage	TLE2161I	V _{IC} = 0, R _S = 50 Ω	25°C	0.8 3.1		mV	
			Full range	4.4			
	TLE2161AI		25°C	0.6 2.6			
			Full range	3.9			
	TLE2161BI		25°C	0.5 1.9			
			Full range	2.7			
αV _{IO} Temperature coefficient of input offset voltage			Full range	6		μV/°C	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo	
I _{IO} Input offset current			25°C	1		pA	
			Full range	2		nA	
I _{IB} Input bias current			25°C	3		pA	
			Full range	4		nA	
V _{ICR} Common-mode input voltage range		25°C	–1.6 to 4	–2 to 6	V		
		Full range	–1.6 to 4				
V _{OM} + Maximum positive peak output voltage	R _L = 10 kΩ	25°C	3.5	3.7	V		
		Full range	3.1				
	R _L = 100 Ω	25°C	2.5	3.1			
		Full range	2				
V _{OM} – Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	–3.7	–3.9	V		
		Full range	–3.1				
	R _L = 100 Ω	25°C	–2.5	–2.7			
		Full range	–2				
A _{VD} Large-signal differential voltage amplification	V _O = ±2.8 V, R _L = 10 kΩ	25°C	15	80	V/mV		
		Full range	2				
	V _O = 0 to 2 V, R _L = 100 Ω	25°C	0.75	45			
		Full range	0.5				
	V _O = 0 to –2 V, R _L = 100 Ω	25°C	0.5	3			
		Full range	0.25				
r _i Input resistance		25°C	10 ¹²		Ω		
c _i Input capacitance		25°C	4		pF		
z _O Open-loop output impedance	I _O = 0	25°C	280		Ω		
CMRR Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	65	82	dB		
		Full range	65				
k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±5 V to ± 15 V, R _S = 50 Ω	25°C	75	93	dB		
		Full range	65				
I _{CC} Supply current	V _O = 0, No load	25°C	280	325	μA		
		Full range	350				
ΔI _{CC} Supply-current change over operating temperature range			Full range	29		μA	

[†] Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{CC} \pm = \pm 5 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLE2161, TLE2161AI TLE2161BI			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C	7	10		V/ μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20 \text{ }\Omega$, $f = 10 \text{ Hz}$	25°C		59	100	nV/ $\sqrt{\text{Hz}}$
		$R_S = 20 \text{ }\Omega$, $f = 1 \text{ kHz}$			43	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$	25°C		1.1		μV
I_n	Equivalent input noise current	$f = 1 \text{ kHz}$	25°C		1		fA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{O(PP)} = 2 \text{ V}$, $R_L = 10 \text{ k}\Omega$, $A_{VD} = 5$, $f = 10 \text{ kHz}$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C		5.8		MHz
		$f = 100 \text{ kHz}$, $R_L = 100 \text{ }\Omega$, $C_L = 100 \text{ pF}$			4.3		
t_s	Settling time	$\epsilon = 0.1\%$	25°C		5		μs
		$\epsilon = 0.01\%$			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10 \text{ k}\Omega$	25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	25°C		70°		
		$A_{VD} = 5$, $R_L = 100 \text{ }\Omega$, $C_L = 100 \text{ pF}$			84°		

[†] Full range is – 40°C to 85°C.

TLE2161, TLE2161A, TLE2161B
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE
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electrical characteristics at specified free-air temperature, $V_{CC} \pm \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2161I, TLE2161AI TLE2161BI			UNIT
				MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	0.6		3	mV
			Full range	4.3			
			25°C	0.5		1.5	
			Full range	2.9			
			25°C	0.3		0.5	
			Full range	1.3			
α _{VIO}	Temperature coefficient of input offset voltage			Full range	6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo
I _{IO}	Input offset current			25°C	2		pA
				Full range	3		nA
I _{IB}	Input bias current		25°C	4		pA	
			Full range	5		nA	
V _{ICR}	Common-mode input voltage range		25°C	–11 to 13	–12 to 16	V	
			Full range	–11 to 13		V	
V _{OM} +	Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	13.2	13.7	V	
			Full range	13			
		R _L = 600 Ω	25°C	12.5	13.2		
			Full range	12			
V _{OM} –	Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	–13.2	–13.7	V	
			Full range	–13			
		R _L = 600 Ω	25°C	–12.5	–13		
			Full range	–12			
A _{VD}	Large-signal differential voltage amplification	V _O = ±10 V, R _L = 10 kΩ	25°C	30	230	V/mV	
			Full range	20			
		V _O = 0 to 8 V, R _L = 600 Ω	25°C	25	100		
			Full range	10			
		V _O = 0 to – 8 V, R _L = 600 Ω	25°C	3	25		
			Full range	1			
r _i	Input resistance		25°C	10 ¹²		Ω	
c _i	Input capacitance		25°C	4		pF	
z _O	Open-loop output impedance	I _O = 0	25°C	280		Ω	
CMRR	Common-mode rejection ratio	V _{IC} =V _{ICRmin} , R _S = 50 Ω	25°C	72	90	dB	
			Full range	65			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±5 V to ±15 V, R _S = 50 Ω	25°C	75	93	dB	
			Full range	65			
I _{CC}	Supply current	V _O = 0, No load	25°C	290	350	μA	
			Full range	375			
ΔI _{CC}	Supply-current change over operating temperature range			Full range	34		μA

† Full range is -40°C to 85°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



operating characteristics at specified free-air temperature, $V_{CC} \pm = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLE2161, TLE2161A TLE2161B			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	7	10		V/ μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20\text{ }\Omega$, $f = 10\text{ Hz}$	25°C		70	100	nV/ $\sqrt{\text{Hz}}$
		$R_S = 20\text{ }\Omega$, $f = 1\text{ kHz}$			40	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		μV
I_n	Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1.1		fA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{O(PP)} = 2\text{ V}$, $A_{VD} = 5$, $f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	$f = 100\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		6.4		MHz
		$f = 100\text{ kHz}$, $R_L = 600\text{ }\Omega$, $C_L = 100\text{ pF}$			5.6		
t_s	Settling time	$\epsilon = 0.1\%$	25°C		5		μs
		$\epsilon = 0.01\%$			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10\text{ k}\Omega$	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		72°		
		$A_{VD} = 5$, $R_L = 600\text{ }\Omega$, $C_L = 100\text{ pF}$			78°		

[†] Full range is – 40°C to 85°C.

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electrical characteristics at specified free-air temperature, $V_{CC} \pm \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2161M TLE2161AM TLE2161BM		UNIT	
				MIN	TYP		MAX
V _{IO}	Input offset voltage	TLE2161M	25°C	0.8	3.1	mV	
			Full range	6			
			TLE2161AM	25°C	0.6		2.6
				Full range	4.6		
			TLE2161BM	25°C	0.5		1.9
				Full range	3.1		
αV _{IO}	Temperature coefficient of input offset voltage	V _{IC} = 0, R _S = 50 Ω	Full range	6		μV/°C	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo	
I _{IO}	Input offset current		25°C	1		pA	
			Full range	15		nA	
I _{IB}	Input bias current		25°C	3		pA	
			Full range	30		nA	
V _{ICR}	Common-mode input voltage range		25°C	−1.6 to 4	−2 to 6	V	
			Full range	−1.6 to 4		V	
V _{OM} +	Maximum positive peak output voltage swing	All packages	25°C	3.5	3.7	V	
			Full range	3			
		FK and JG packages	25°C	2.5	3.6	V	
			Full range	2			
		D and P packages	25°C	2.5	3.1		
			Full range	2			
V _{OM} −	Maximum negative peak output voltage swing	All packages	25°C	−3.7	−3.9	V	
			Full range	−3			
		FK and JG packages	25°C	−2.5	−3.5		
			Full range	−2			
		D and P packages	25°C	−2.5	−2.7		
			Full range	−2			
A _{VD}	Large-signal differential voltage amplification	All packages	25°C	15	80	V/mV	
			Full range	2			
		FK and JG packages	25°C	1	65		
			Full range	0.5			
			25°C	1	16		
			Full range	0.5			
		D and P packages	25°C	0.75	45		
			Full range	0.5			
			25°C	0.5	3		
			Full range	0.25			

† Full range is -55°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



electrical characteristics at specified free-air temperature, $V_{CC} \pm = \pm 5$ V (unless otherwise noted continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2161M TLE2161AM TLE2161BM			UNIT
			MIN	TYP	MAX	
r_i Input resistance		25°C		10 ¹²		Ω
c_i Input capacitance		25°C		4		pF
z_o Open-loop output impedance	$I_O = 0$	25°C		280		Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C	65	82		dB
		Full range	60			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50 \Omega$	25°C	75	93		dB
		Full range	65			
I_{CC} Supply current	$V_O = 0,$ No load	25°C		280	325	μA
		Full range			350	
ΔI_{CC} Supply-current change over operating temperature range		Full range		39		μA

[†] Full range is –55°C to 125°C.

operating characteristics, $V_{CC} \pm = \pm 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2161M TLE2161AM TLE2161BM			UNIT
		MIN	TYP	MAX	
SR Slew rate (see Figure 1)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		10		V/μs
V_n Equivalent input noise voltage (see Figure 2)	$R_S = 20 \Omega, f = 10 \text{ Hz}$		59		nV/√Hz
	$R_S = 20 \Omega, f = 1 \text{ kHz}$		43		
$V_{n(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$		1.1		μV
I_n Equivalent input noise current	$f = 1 \text{ kHz}$		1		fA/√Hz
THD Total harmonic distortion	$A_{VD} = 5, V_{O(PP)} = 2 \text{ V}, f = 10 \text{ kHz}, R_L = 10 \text{ k}\Omega$		0.025%		
Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		5.8		MHz
	$f = 100 \text{ kHz}, R_L = 600 \text{ k}\Omega, C_L = 100 \text{ pF}$		4.3		
t_s Settling time	$\epsilon = 0.1\%$		5		μs
	$\epsilon = 0.01\%$		10		
BOM Maximum output-swing bandwidth	$A_{VD} = 5, R_L = 10 \text{ k}\Omega$		420		kHz
ϕ_m Phase margin (see Figure 3)	$A_{VD} = 5, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$		70°		
	$A_{VD} = 5, R_L = 600 \Omega, C_L = 100 \text{ pF}$		84°		

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electrical characteristics at specified free-air temperature, $V_{CC} \pm = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2161M TLE2161AM TLE2161BM			UNIT
				MIN	TYP	MAX	
V _{IO}	Input offset voltage	TLE2161M	25°C	0.6	3	mV	
			Full range	6			
			TLE2161AM	25°C	0.5		1.5
				Full range	3.6		
			TLE2161BM	25°C	0.3		0.5
				Full range	1.7		
α _{VIO}	Temperature coefficient of input offset voltage	V _{IC} = 0, R _S = 50 Ω	Full range	6		μV/°C	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo	
I _{IO}	Input offset current		25°C	2		pA	
			Full range	20		nA	
I _{IB}	Input bias current		25°C	4		pA	
			Full range	40		nA	
V _{ICR}	Common-mode input voltage range		25°C	−11 to 13	−12 to 16	V	
			Full range	−11 to 13		V	
V _{OM} +	Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	13.2	13.7	V	
			Full range	12.5			
		R _L = 600 Ω	25°C	12.5	13.2		
			Full range	12			
V _{OM} −	Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	−13.2	−13.7	V	
			Full range	−12.5			
		R _L = 600 Ω	25°C	−12.5	−13		
			Full range	−12			
A _{VD}	Large-signal differential voltage amplification	V _O = ±10 V, R _L = 10 kΩ	25°C	30	230	V/mV	
			Full range	20			
		V _O = 0 to 8 V, R _L = 600 Ω	25°C	25	100		
			Full range	7			
		V _O = 0 to − 8 V, R _L = 600 Ω	25°C	3	25		
			Full range	1			
r _i	Input resistance		25°C	10 ¹²		Ω	
c _i	Input capacitance		25°C	4		pF	
z _o	Open-loop output impedance	I _O = 0	25°C	280		Ω	
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	72	90	dB	
			Full range	65			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±5 V to ±15 V, R _S = 50 Ω	25°C	75	93	dB	
			Full range	65			
I _{CC}	Supply current	V _O = 0, No load	25°C	290	350	μA	
			Full range	375			
ΔI _{CC}	Supply-current change over operating temperature range			Full range	46		μA

[†] Full range is –55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

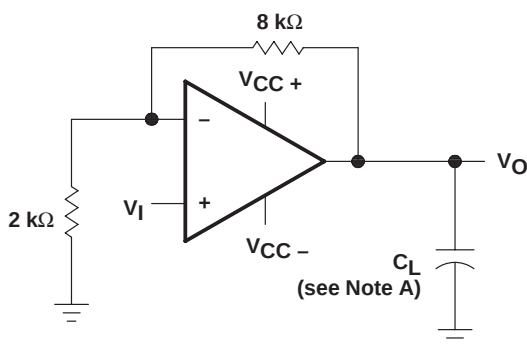


operating characteristics at specified free-air temperature, $V_{CC} \pm \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2161M TLE2161AM TLE2161BM			UNIT
			MIN	TYP	MAX	
SR Slew rate (see Figure 1)	$A_{VD} = 5, \quad R_L = 10 \text{ k}\Omega, \quad C_L = 100 \text{ pF}$	25°C	7	10		V/ μ s
		Full range	5			
V_n Equivalent input noise voltage (see Figure 2)	$R_S = 20 \text{ }\Omega, \quad f = 10 \text{ Hz}$	25°C		70		nV/ $\sqrt{\text{Hz}}$
	$R_S = 20 \text{ }\Omega, \quad f = 1 \text{ kHz}$			40		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$	25°C		1.1		μ V
I_n Equivalent input noise current	$f = 1 \text{ Hz}$	25°C		1.1		fA/ $\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{O(PP)} = 2 \text{ V}, \quad A_{VD} = 5, \quad f = 10 \text{ kHz},$ $R_L = 10 \text{ k}\Omega$	25°C		0.025%		
Gain-bandwidth product (see Figure 3)	$f = 100 \text{ kHz}, \quad R_L = 10 \text{ k}\Omega, \quad C_L = 100 \text{ pF}$	25°C		6.4		MHz
	$f = 100 \text{ kHz}, \quad R_L = 600 \text{ }\Omega, \quad C_L = 100 \text{ pF}$			5.6		
t_s Settling time	$\epsilon = 0.1\%$	25°C		5		μ s
	$\epsilon = 0.01\%$			10		
B_{OM} Maximum output-swing bandwidth	$A_{VD} = 5, \quad R_L = 10 \text{ k}\Omega$	25°C		116		kHz
ϕ_m Phase margin (see Figure 3)	$A_{VD} = 5, \quad R_L = 10 \text{ k}\Omega, \quad C_L = 100 \text{ pF}$	25°C		72°		
	$A_{VD} = 5, \quad R_L = 600 \text{ }\Omega, \quad C_L = 100 \text{ pF}$			78°		

[†] Full range is – 55°C to 125°C.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

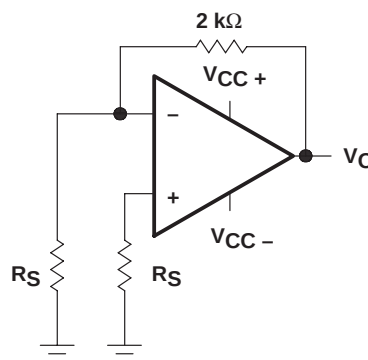
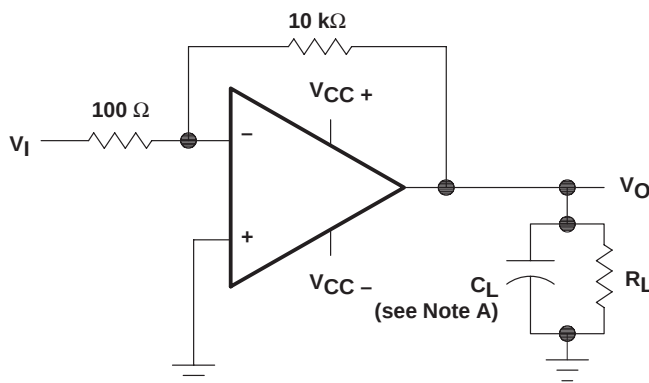


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Gain-Bandwidth Product and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

Input bias and offset current

At the picoampere bias-current level typical of the TLE2161, TLE2161A, and TLE2161B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5 6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{ICR}	Common-mode input voltage range limits	vs Free-air temperature	7
V_{OM}	Maximum positive peak output voltage	vs Output current	8
V_{OM}	Maximum negative peak output voltage	vs Output current	9
V_{OM}	Maximum peak output voltage	vs Supply voltage	10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	16 17
I_{OS}	Short-circuit output current	vs Elapsed time	18
	Large-signal voltage amplification	vs Free-air temperature	19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	22 23
	Pulse response	Small signal Large signal	24, 25 26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
V_n	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	32 33
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature	34 35
	Phase shift	vs Frequency	16

TYPICAL CHARACTERISTICS†

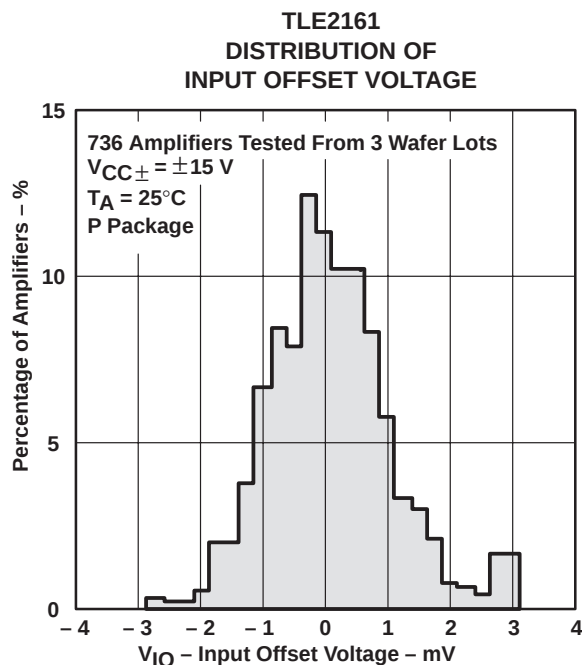


Figure 4

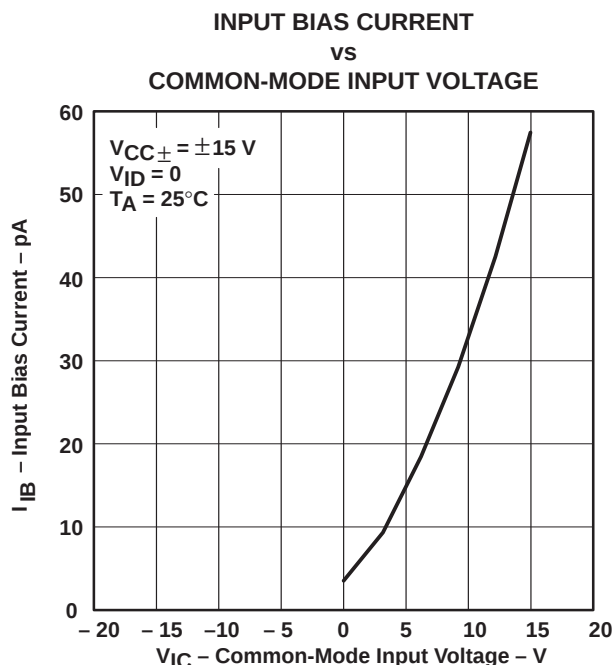


Figure 5

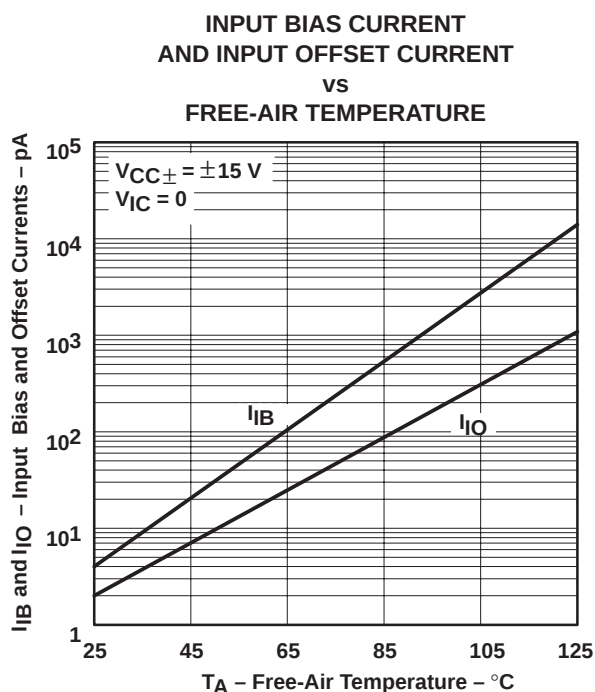


Figure 6

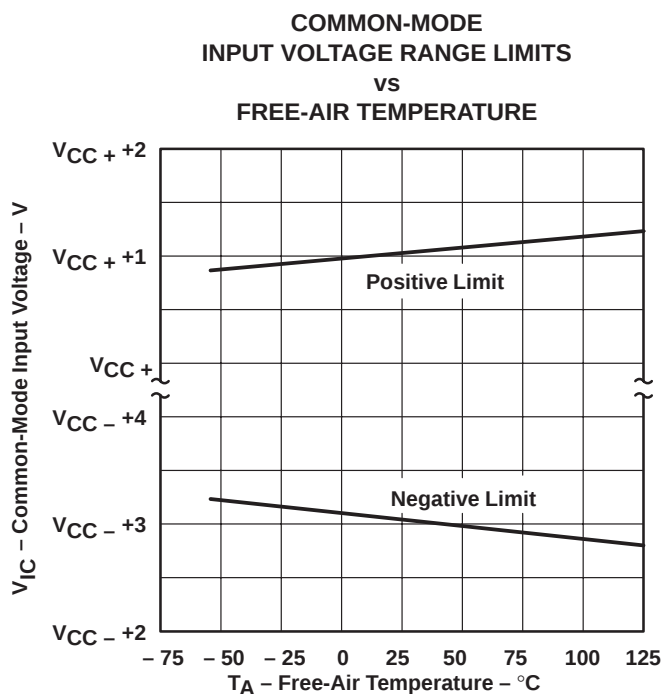


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

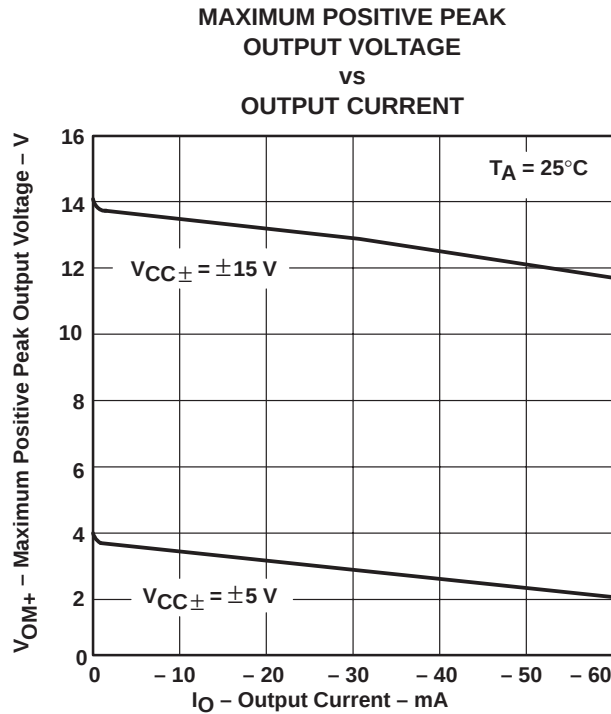


Figure 8

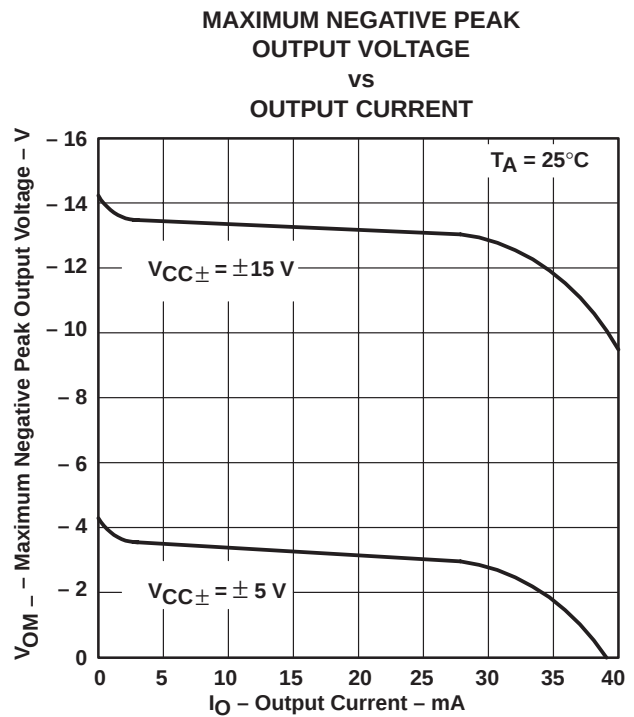


Figure 9

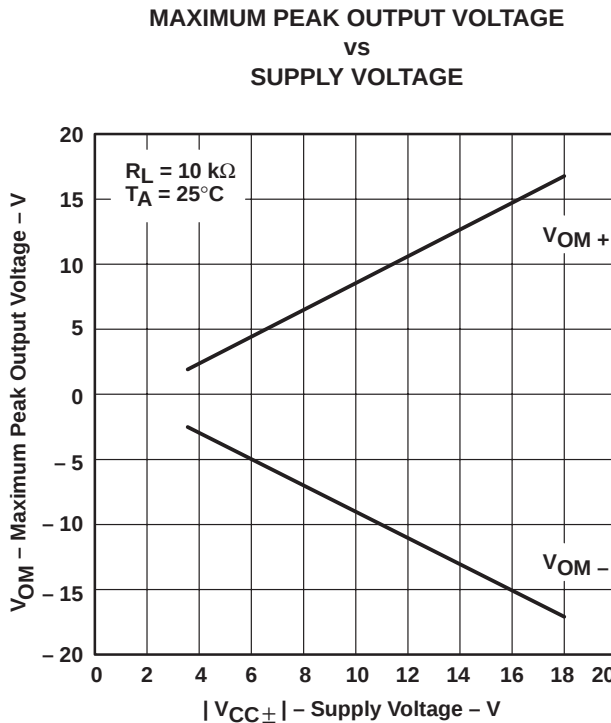


Figure 10

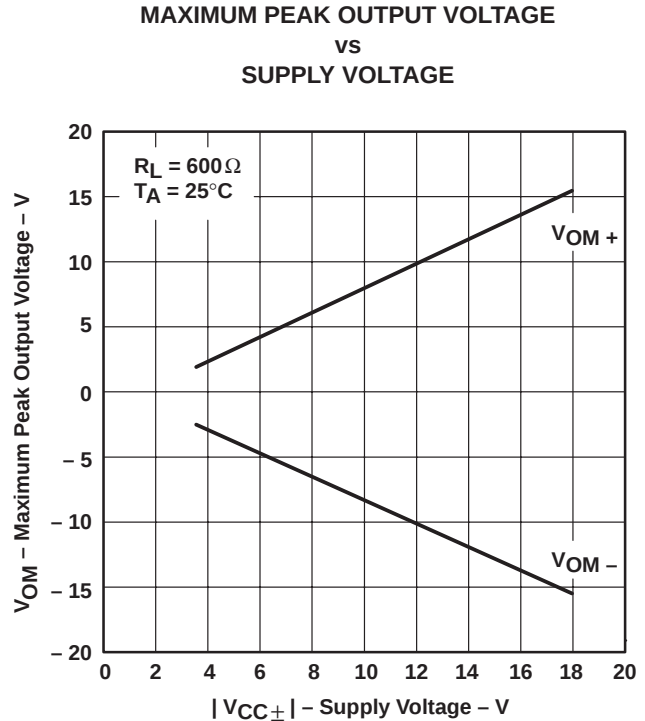


Figure 11

TYPICAL CHARACTERISTICS

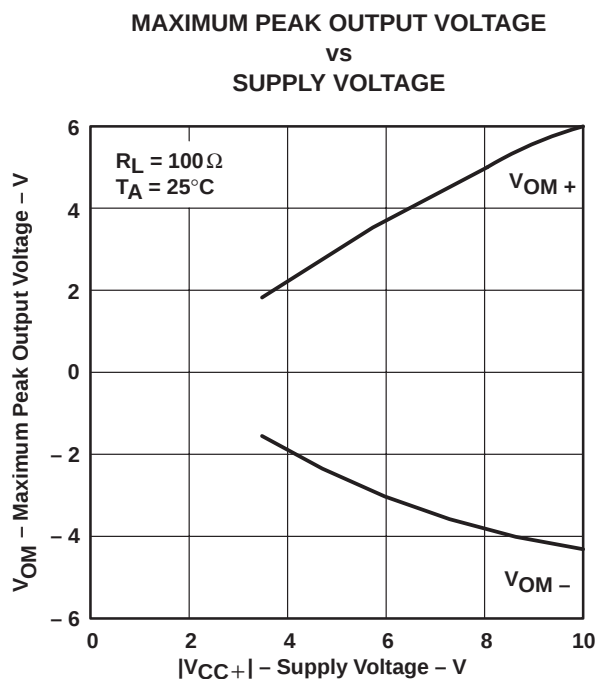


Figure 12

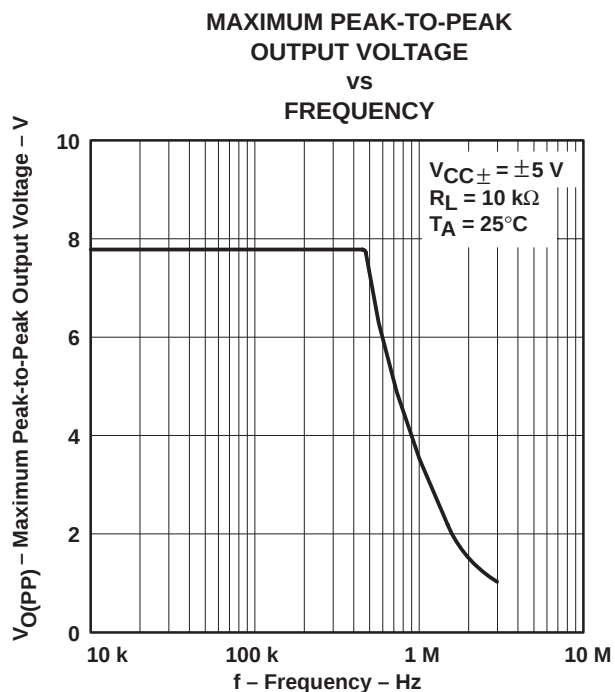


Figure 13

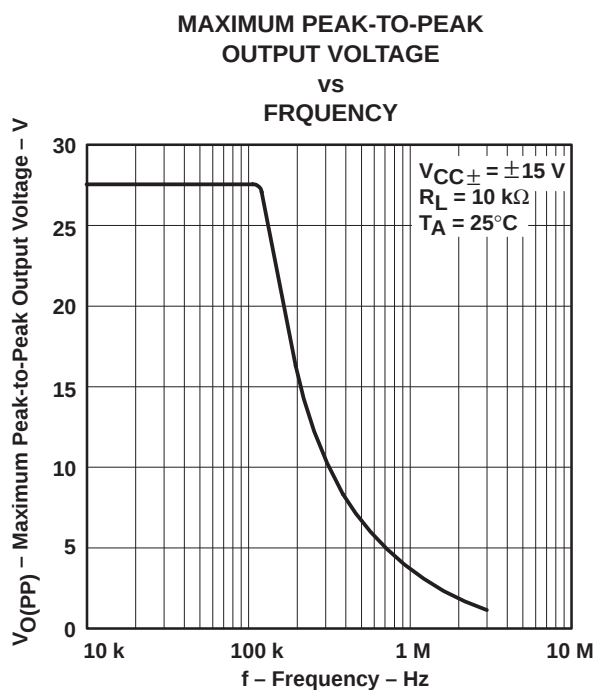


Figure 14

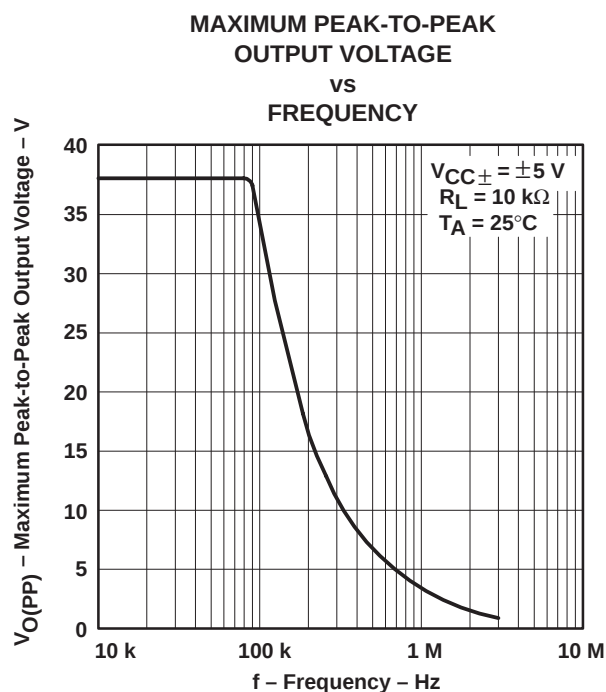
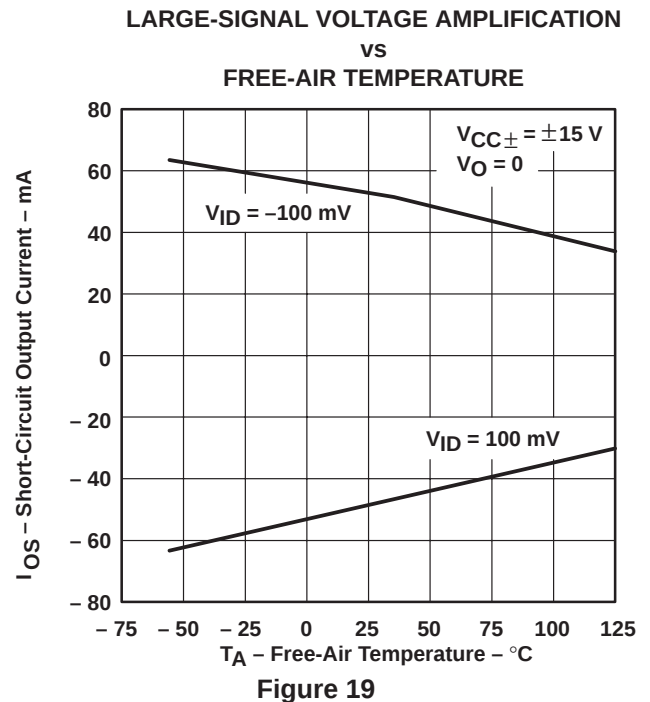
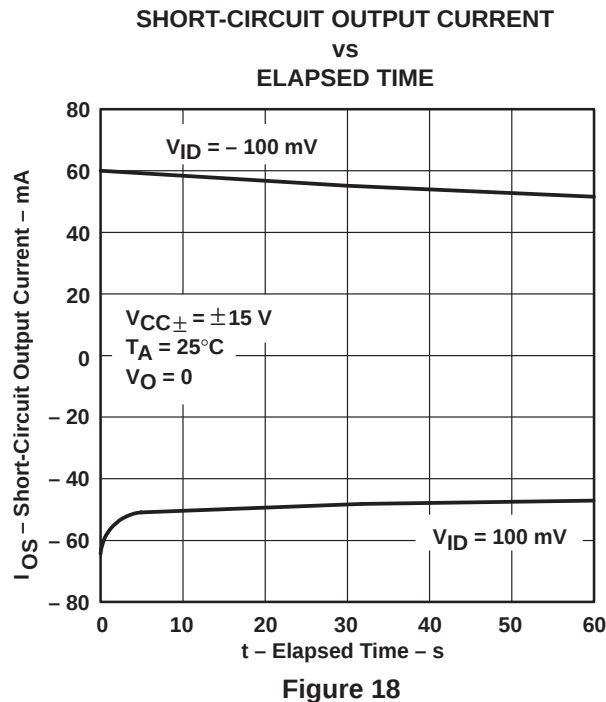
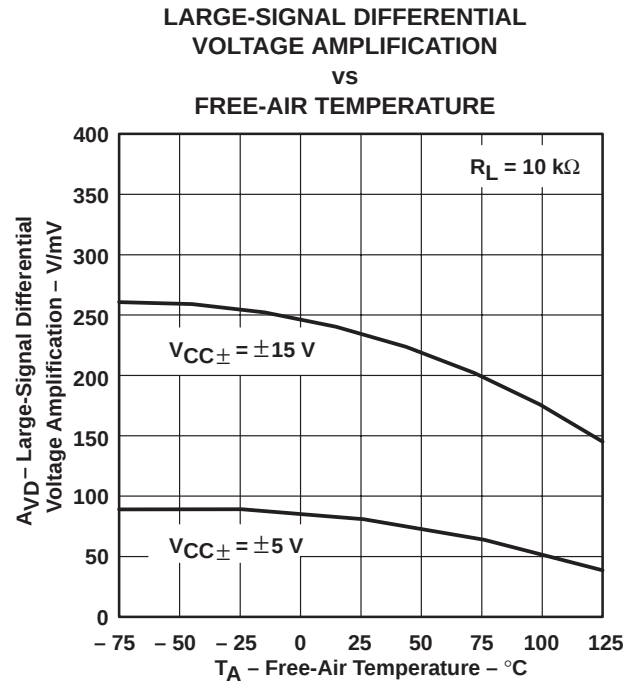
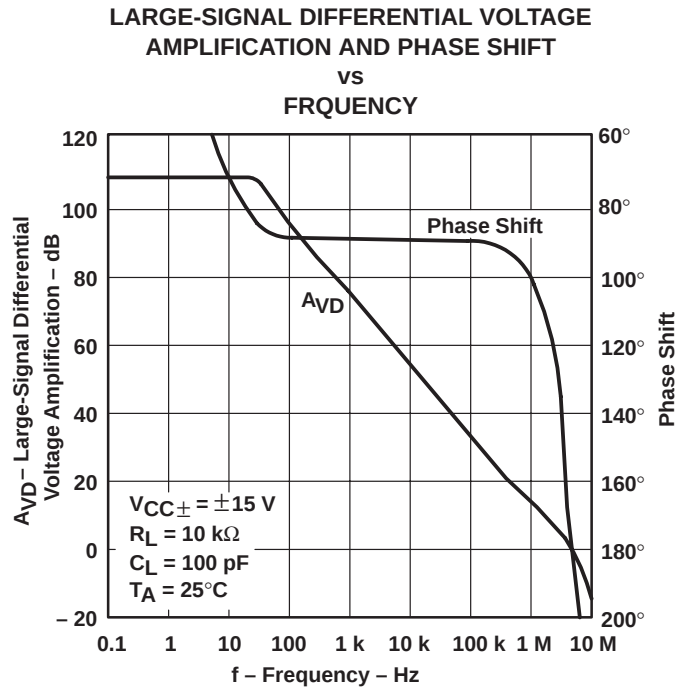


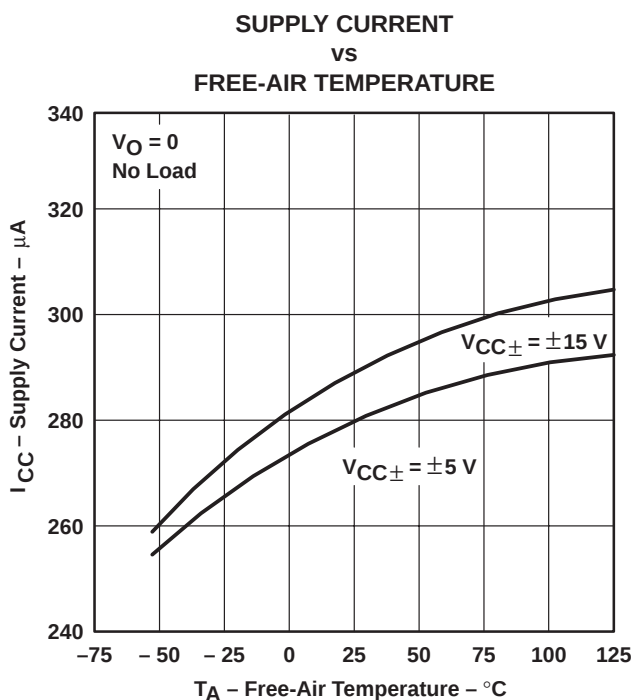
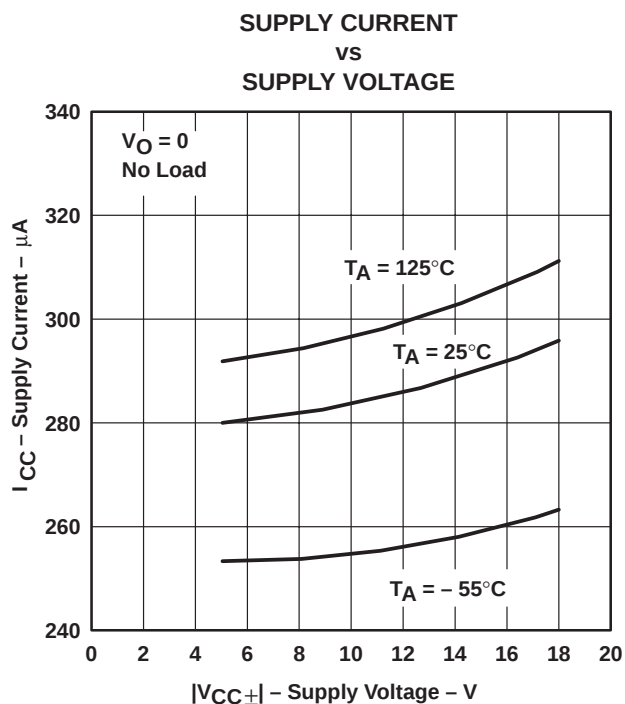
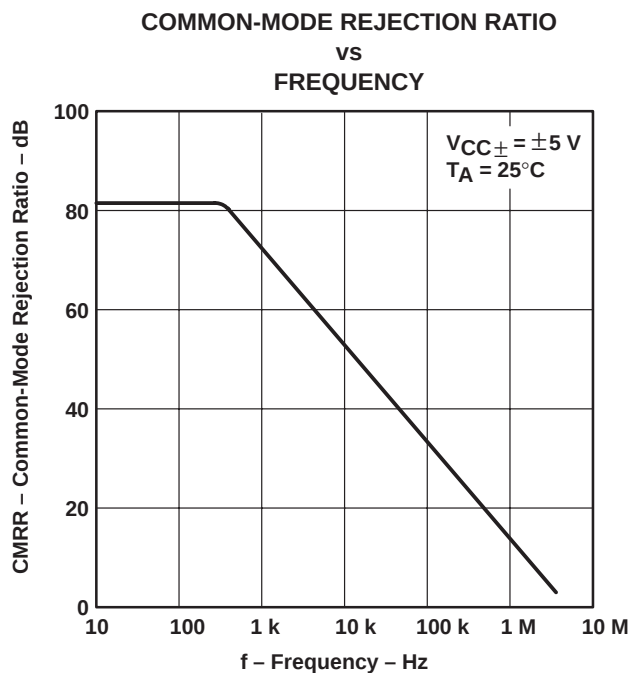
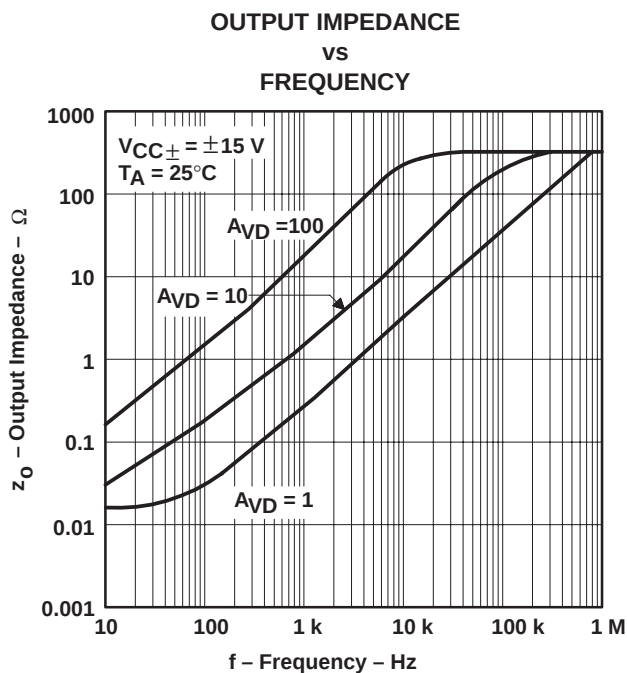
Figure 15

TYPICAL CHARACTERISTICS†



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

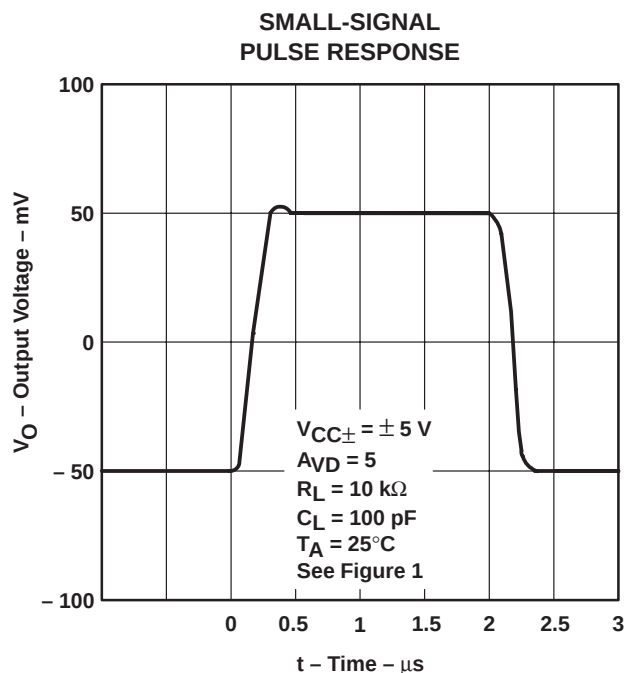


Figure 24

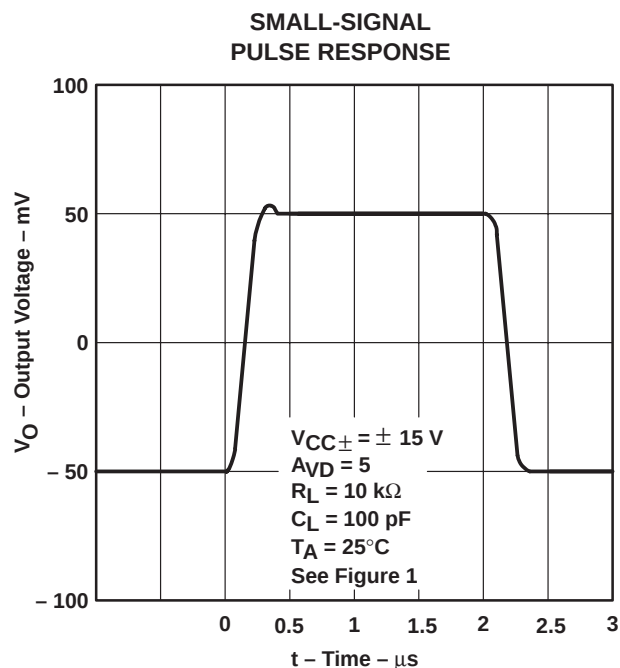


Figure 25

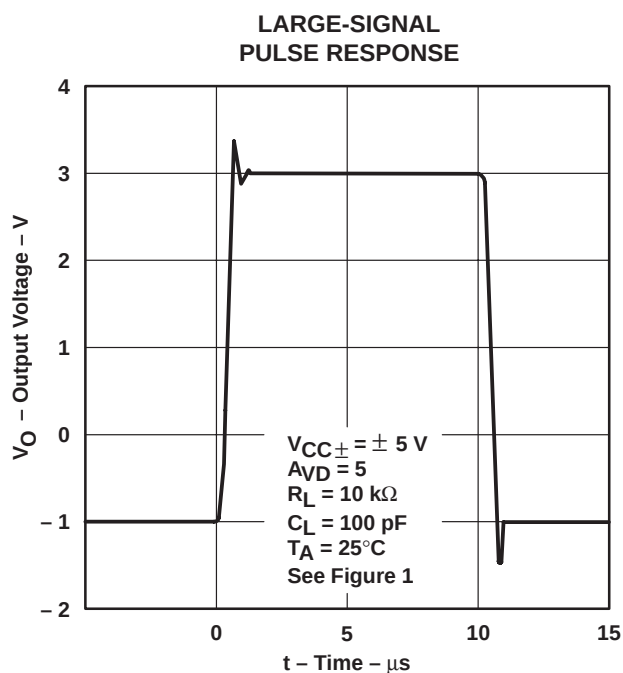


Figure 26

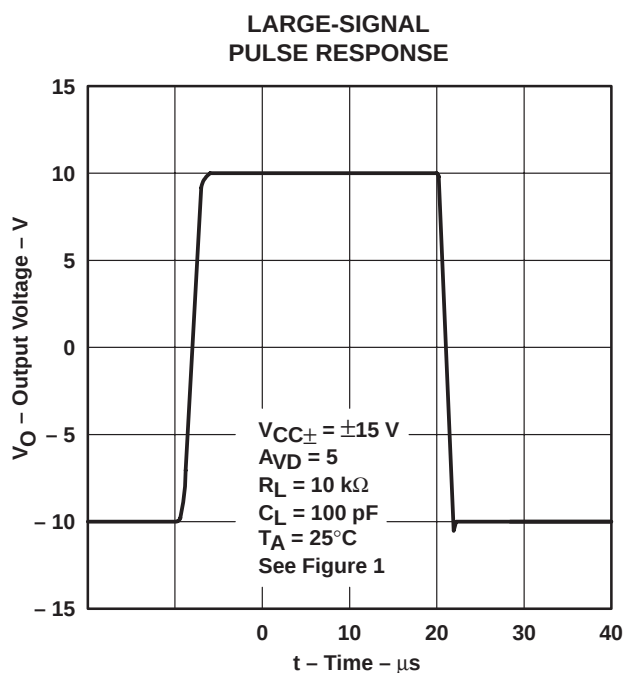


Figure 27

TYPICAL CHARACTERISTICS

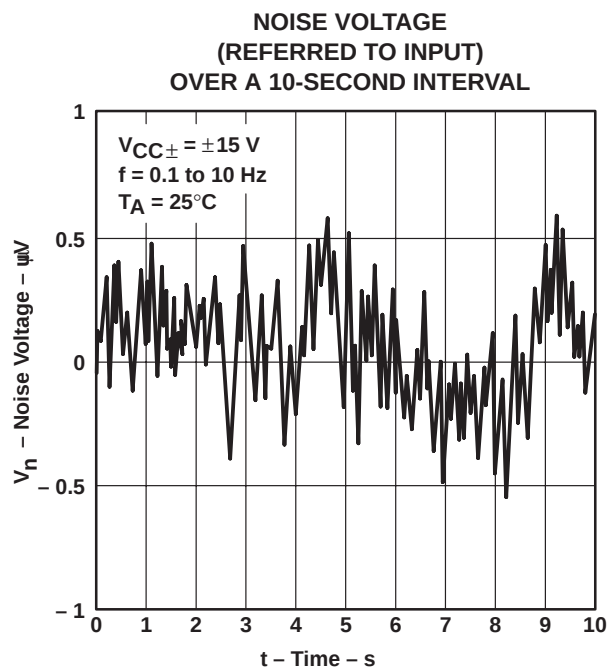


Figure 28

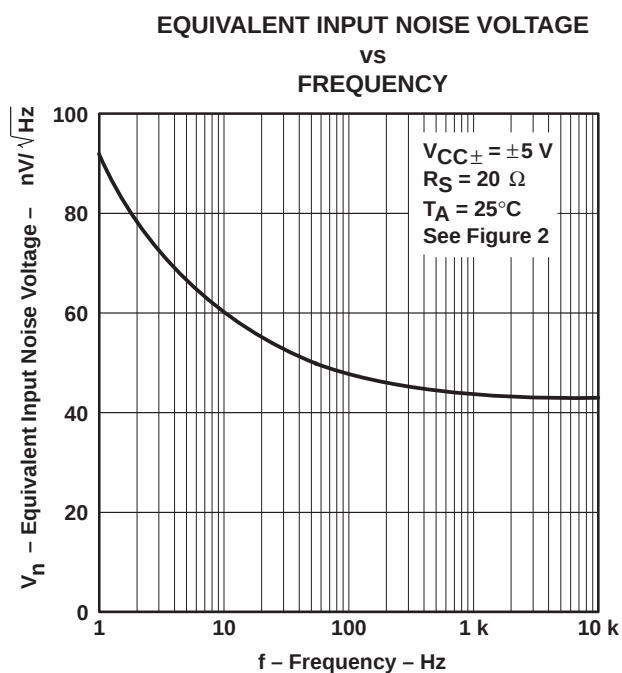


Figure 29

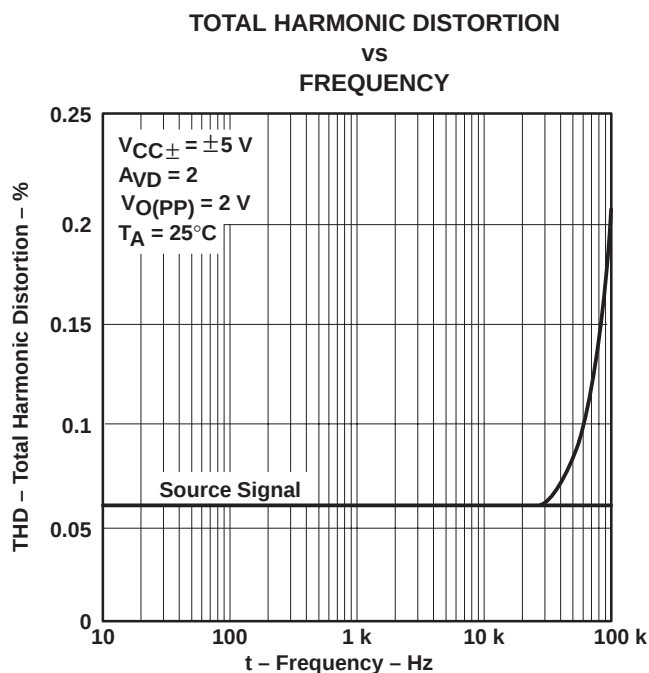


Figure 30

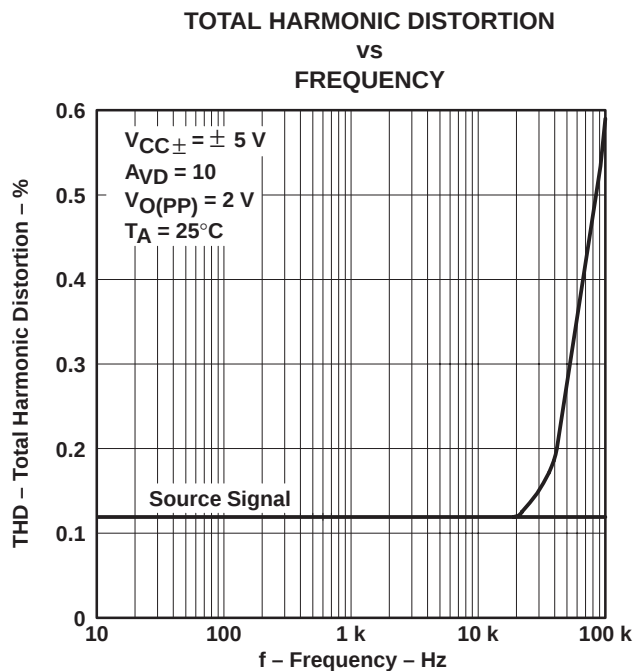


Figure 31

TYPICAL CHARACTERISTICS

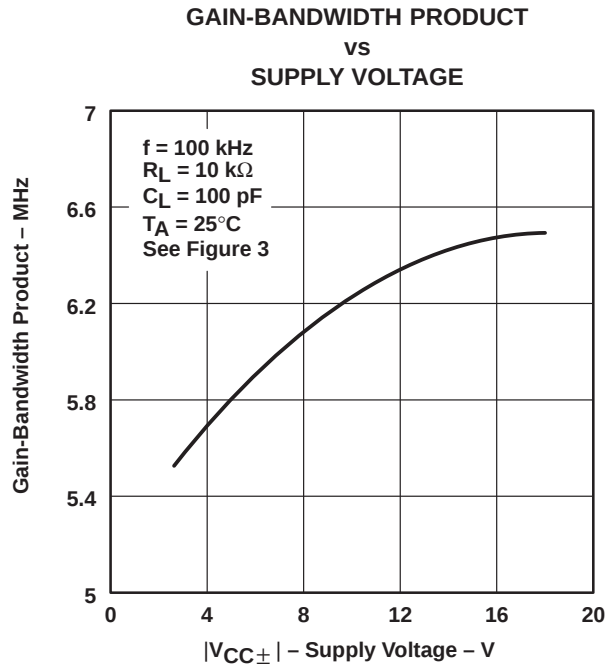


Figure 32

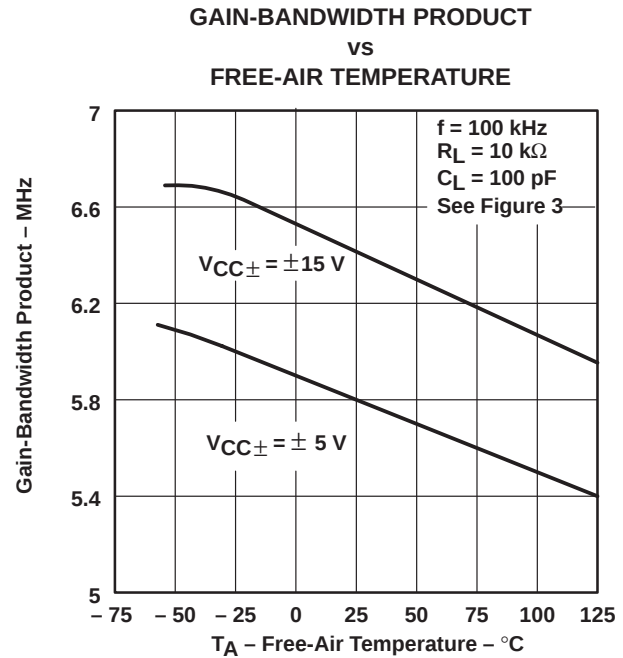


Figure 33

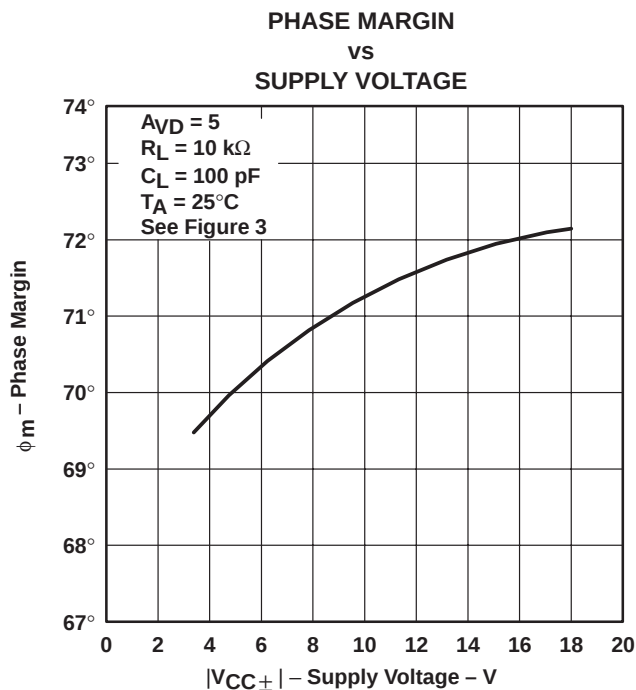


Figure 34

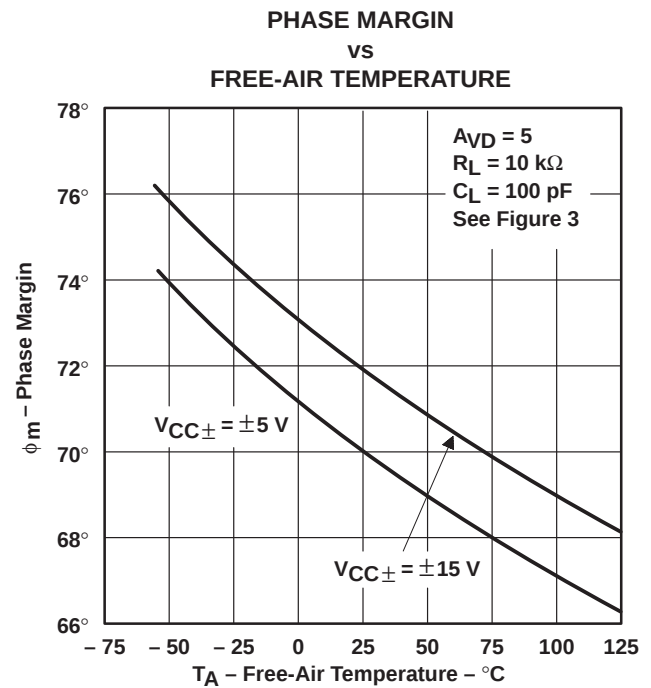


Figure 35

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 36 and Figure 37 were generated using the TLE2161 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

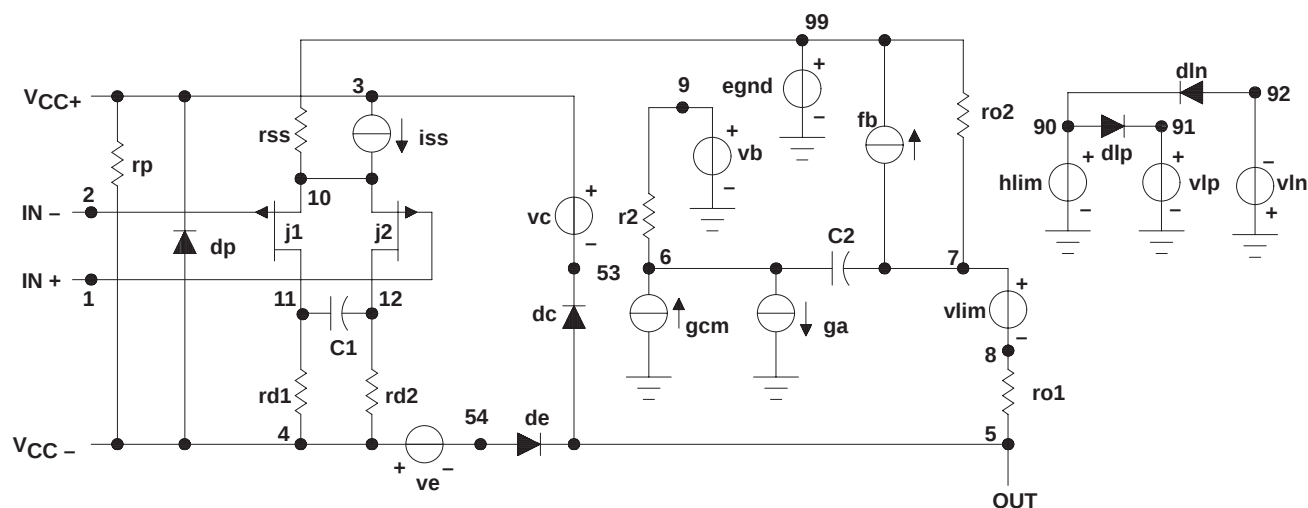


Figure 36. Boyle Macromodel

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2161 1 2 3 4 5
c1      11 12 125.4E-14
c2       6  7  5.000E-12
dc       5 53 dx
de      54 5d x
dlp     90 91 dx
dln     92 90 dx
dp       4  3 dx
egnd    99  0 poly(2) (3,0) (4,0) 0 .5 .5
fb       7 99 poly(5) vb vc ve vlp vln 0 4.085E6 -4E6 4E6 4E6 -4E6
ga       6  0 11 12 201.1E-6
gcm      0  6 10 99 3.576E-9
iss      3 10 dc 45.00E-6
hlim    90  0 vlim 1K
j1      11  2 10 jx
j2      12  1 10 jx
r2       6  9 100.0E3
rd1      4 11 4.973E3
rd2      4 12 4.973E3
ro1      8  5 280
ro2      7 99 280
rp       3  4 113.2E3
rss     10 99 4.444E6
vb       9  0 dc 0
vc       3 53 dc 2
ve      54  4 dc 2
vlim     7  8 dc 0
vlp     91  0 dc 50
vln      0 92 dc 50
.model dx D (Is=800.0E-18)
.model jx PJF (Is=1.000E-12 Beta=480E-6 Vto=-1)
.ends
```

Figure 37. Macromodel Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2161, TLE2161A and TLE2161B are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2161, TLE2161A, and TLE2161B are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

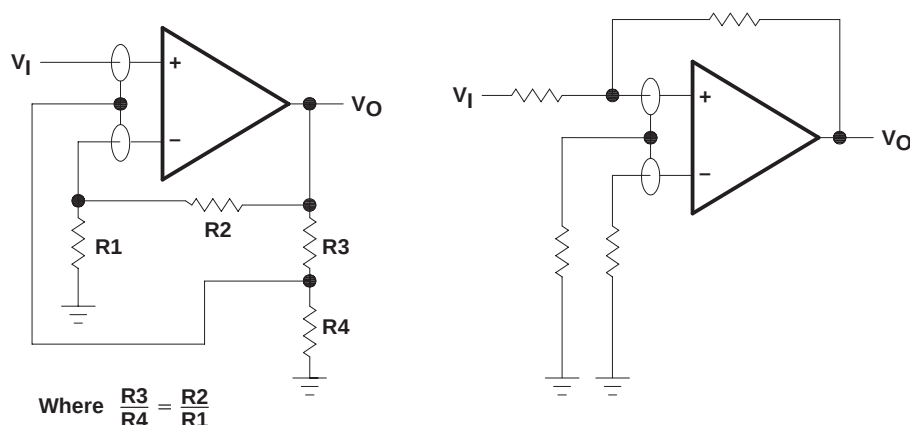


Figure 38. Use of Guard Rings

input offset voltage nulling

The TLE2161 series offers external null pins that can further reduce the input offset voltage. The circuit in Figure 39 can be connected as shown if the feature is desired. When external nulling is not needed, the null pins may be left disconnected.

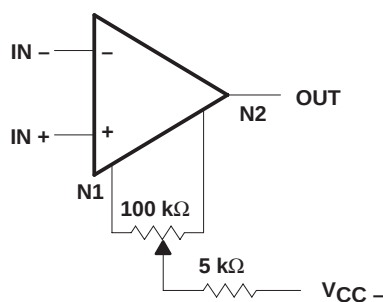


Figure 39. Input Offset Voltage Nulling

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9095801QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9095801QPA TLE2161M	Samples
5962-9095802QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9095802QPA TLE2161AM	Samples
5962-9095803QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9095803QPA TLE2161BM	Samples
TLE2161ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2161AC	Samples
TLE2161AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2161AI	Samples
TLE2161AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2161AI	Samples
TLE2161AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9095802QPA TLE2161AM	Samples
TLE2161BMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9095803QPA TLE2161BM	Samples
TLE2161CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2161C	Samples
TLE2161ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2161I	Samples
TLE2161IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2161I	Samples
TLE2161IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2161I	Samples
TLE2161MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9095801QPA TLE2161M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLE2161, TLE2161A, TLE2161AM, TLE2161M :

- Catalog : [TLE2161A](#), [TLE2161](#)
- Military : [TLE2161M](#), [TLE2161AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

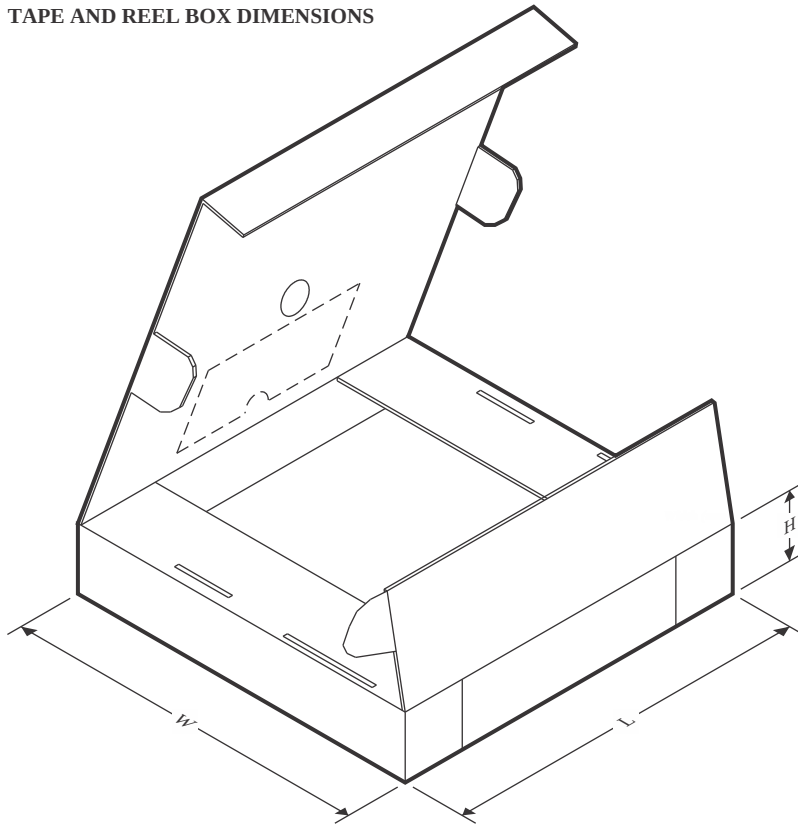
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2161AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2161AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2161IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2161AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2161AIDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2161IDR	SOIC	D	8	2500	340.5	338.1	20.6

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