

## 45 Gbps, 1:4 DEMUX WITH PROGRAMMABLE OUTPUT VOLTAGE

### Typical Applications

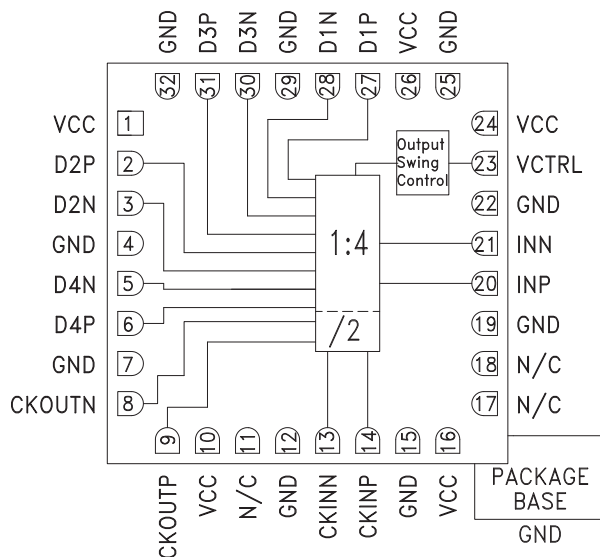
The HMC848LC5 is ideal for:

- SONET OC-768
- RF ATE Applications
- Broadband Test & Measurements
- Serial Data Transmission up to 45 Gbps
- High Speed ADC Interfacing

### Features

- Supports Data Rates up to 45 Gbps
- Half Rate Clock Input
- Quarter Rate Reference Clock Output
- Fast Rise and Fall Times: 25 / 21 ps
- Programmable Differential Output  
Voltage Swing: 300 - 1000 mVp-p
- Single Supply: +3.3V
- 32 Lead Ceramic 5x5 mm SMT Package: 25 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC848LC5 is a 1:4 demultiplexer designed for data deserialization up to 45 Gbps. The device uses both rising and falling edges of the half-rate clock to sample the input data in sequence, D0-D3 and latches the data onto the differential outputs. A quarter-rate clock output generated on-chip can be used to clock the data into other devices.

All clock and data inputs / outputs of the HMC848LC5 are CML and terminated on-chip with 50 Ohms to the VCC, and may be DC or AC coupled. The inputs and outputs of the HMC848LC5 may be operated either differentially or single-ended. The HMC848LC5 also features an output level control pin, VCTRL, which allows for loss compensation or signal level optimization. The HMC848LC5 operates from a single +3.3V supply and is available in ROHS compliant 5x5 mm SMT package.

### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{CC} = 3.3\text{V}$

| Parameter   | Conditions                                | Min. | Typ. | Max  | Units |
|---|---|------|------|------|-------|
| Power Supply Voltage                                  | $\pm 5\%$ Tolerance                       | 3.13 | 3.3  | 3.47 | V     |
| Power Supply Current                                  | $V_{ctrl} = 2.5\text{V}$                  | 480  | 540  | 600  | mA    |
| Output Amplitude Control Voltage Range ( $V_{ctrl}$ ) |   | 1.7  | 2.5  | 3    | V     |
| Maximum Data Rate                                     |   | 45   |      |      | Gbps  |
| Maximum Clock Rate                                    | Half Rate Clock                           | 22.5 |      |      | GHz   |
| Input Amplitude (Data)                                | Single-Ended, peak-to-peak <sup>[1]</sup> | 150  |      | 800  | mVp-p |
|   | Differential, peak-to-peak                | 150  |      | 1000 | mVp-p |
| Input Amplitude (Clock)                               | Single-Ended, peak-to-peak <sup>[1]</sup> | 100  |      | 700  | mVp-p |
|   | Differential, peak-to-peak                | 100  |      | 1000 | mVp-p |

[1] The un-used port is biased @ 3.3V

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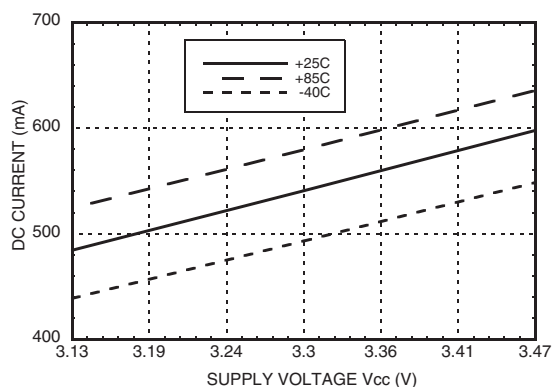
### Electrical Specifications, (continued)

| Parameter   | Conditions                              | Min. | Typ. | Max  | Units  |
|---|---|------|------|------|--------|
| Input High Voltage (Data & Clock)                         | Vctrl = 2.5V                            | 2.8  |      | 3.8  | V      |
| Input Low Voltage (Data & Clock)                          | Vctrl = 2.5V                            | 2.3  |      | 3.3  | V      |
| Data Output Voltage Swing Range                           | Differential, peak-to-peak<br>@ 40 Gbps | 300  |      | 1000 | mVp-p  |
| Clock Output Voltage Swing                                | Differential, peak-to-peak<br>@ 10 GHz  | 600  | 700  | 800  | mVp-p  |
| Output High Voltage                                       | Vctrl = 2.5V                            |      | 2.95 |      | V      |
| Output Low Voltage  | Vctrl = 2.5V                            |      | 2.6  |      | V      |
| Input Return Loss   | Data input up to 11.25 GHz              |      | 10   |      | dB     |
|   | Clock input up to 22.5 GHz              |      | 9    |      | dB     |
| Output Return Loss  | Data output up to 22.5 GHz              |      | 8    |      | dB     |
|   | Clock output up to 11.25 GHz            |      | 8    |      | dB     |
| Deterministic Jitter, Jd [2]                              |   |      | 4    |      | ps p-p |
| Additive Random Jitter, Jr [3]                            |   |      | 0.35 |      | ps rms |
| Rise Time, tr [2]   | 20% - 80%                               |      | 25   |      | ps     |
| Fall Time, tf [2]   | 20% - 80%                               |      | 21   |      | ps     |
| Propagation Delay Clock to Data, Td <sub>pd</sub>         | Input clock to output data              |      | 380  |      | ps     |
| Propagation Delay Clock to Output Clock, Tc <sub>pd</sub> | Input clock to output clock             |      | 80   |      | ps     |
| Set Up Time, ts   | Both at rising and falling edges        |      | 20   |      | ps     |
| Hold Time, th   | Both at rising and falling edges        |      | 2    |      | ps     |

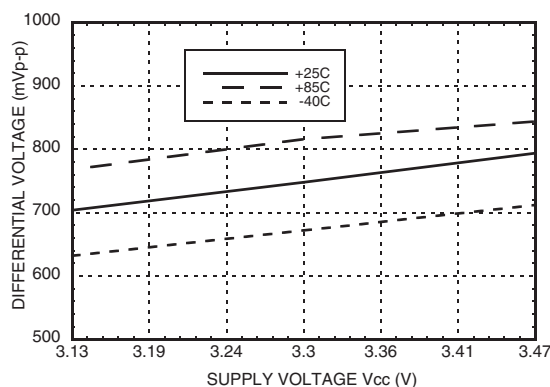
[2] CKINP: 20 GHz clock signal, 250 mVp-p single-ended, INP: 40 Gbps PRBS 2<sup>23</sup>-1 pattern, 250 mVp-p single-ended

[3] Random jitter is measured with 40 Gbps 10101... pattern

**DC Current vs. Supply Voltage [1] [2]**



**Differential Output Swing vs. Supply Voltage [1] [2]**

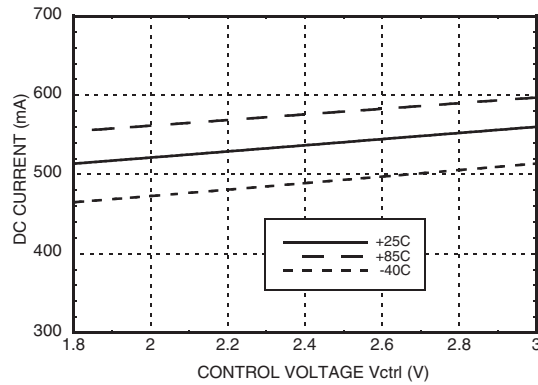


[1] Vctrl = 2.5V

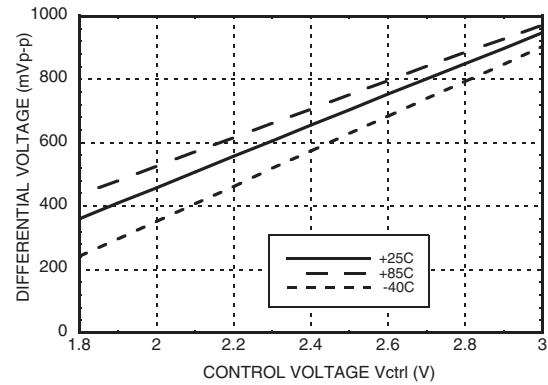
[2] Data Rate = 40 Gbps

## 45 Gbps, 1:4 DEMUX WITH PROGRAMMABLE OUTPUT VOLTAGE

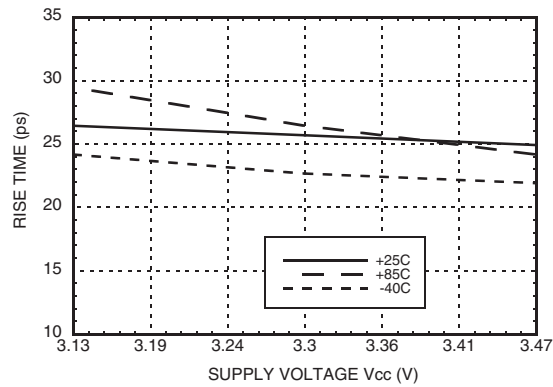
**DC Current vs. Vctrl [1]**



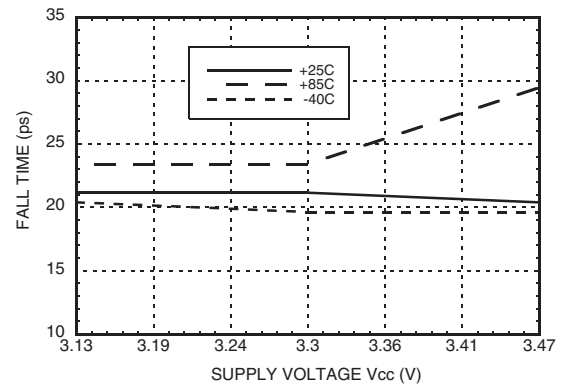
**Differential Output Swing vs. Vctrl [1]**



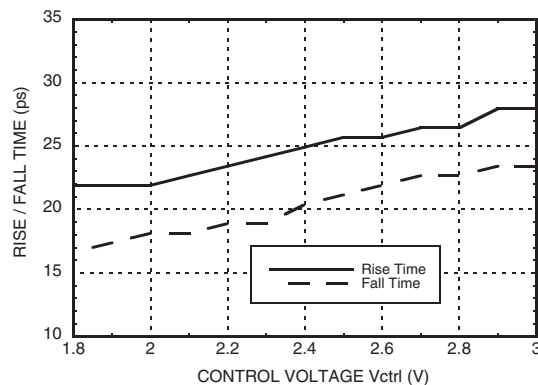
**Rise Time vs. Supply Voltage [1][2][3][4]**



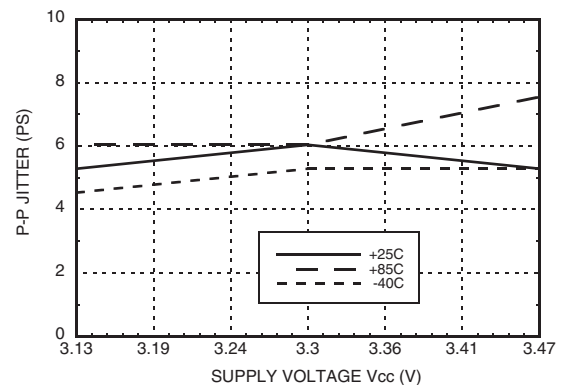
**Fall Time vs. Supply Voltage [1][2][3][4]**



**Rise Time vs. Vctrl [1][3][4]**



**Peak-to-Peak Jitter vs. Supply Voltage [1][2][3][5]**



[1] Data Rate = 40 Gbps

[2] Vctrl = 2.5V

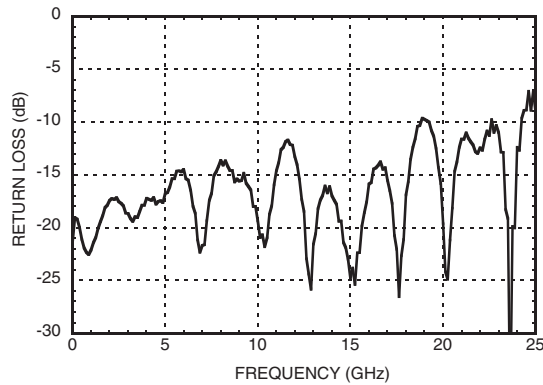
[3] Data was taken at single-ended output

[4] 20% - 80%

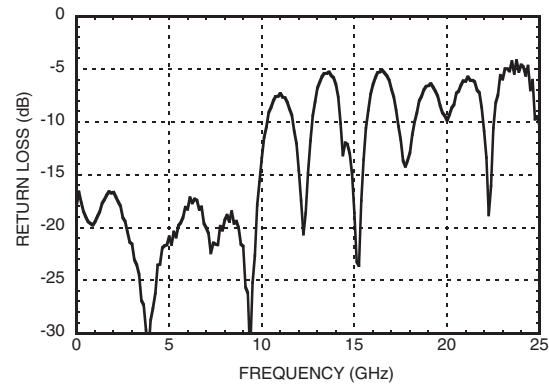
[5] Source jitter was not deembedded

## 45 Gbps, 1:4 DEMUX WITH PROGRAMMABLE OUTPUT VOLTAGE

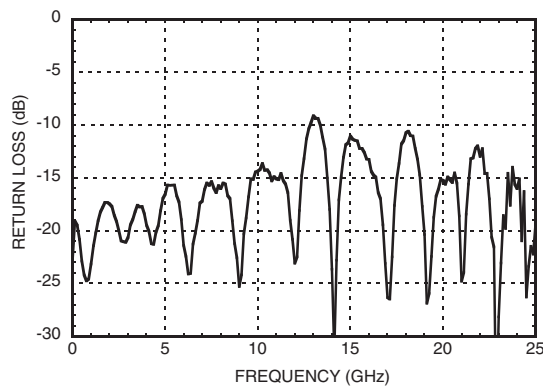
**Data Input Return Loss vs. Frequency [1][2]**



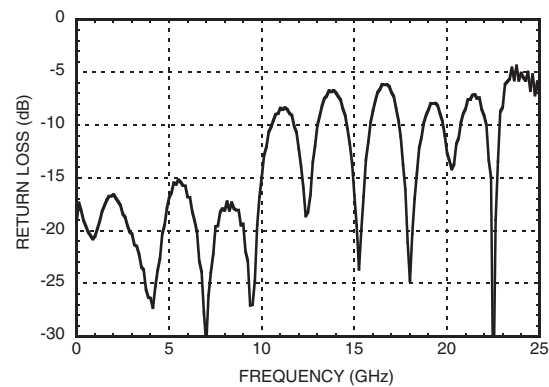
**Data Output Return Loss vs. Frequency [1][2]**



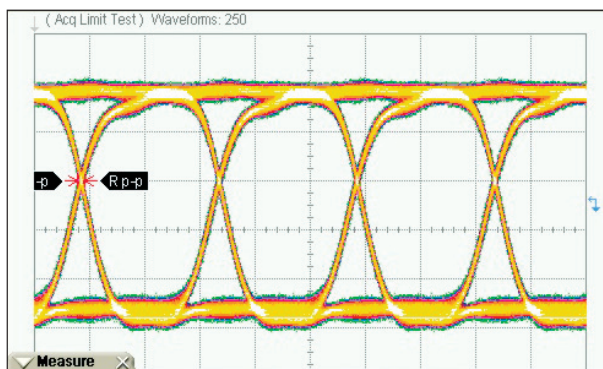
**Clock Input Return Loss vs. Frequency [1][2]**



**Clock Output Return Loss vs. Frequency [1][2]**



**10 Gbps Single-Ended Output Eye Diagram**



| Measurements |         |         |         |             |
|--------------|---------|---------|---------|-------------|
|              | Current | Minimum | Maximum | Total Meas. |
| Eye Amp      | 356 mV  | 356 mV  | 356 mV  | 84          |
| Rise Time    | 25.8 ps | 25.8 ps | 26.7 ps | 84          |
| Fall Time    | 21.3 ps | 21.3 ps | 21.3 ps | 84          |
| p-p jitter   | 5.33 ps | 4.44ps  | 5.33 ps | 84          |

Time Scale: 40 ps/div

Amplitude Scale: 79.7 mV/div

Test Conditions:

VCC = +3.3V, VCTRL = 2.5V

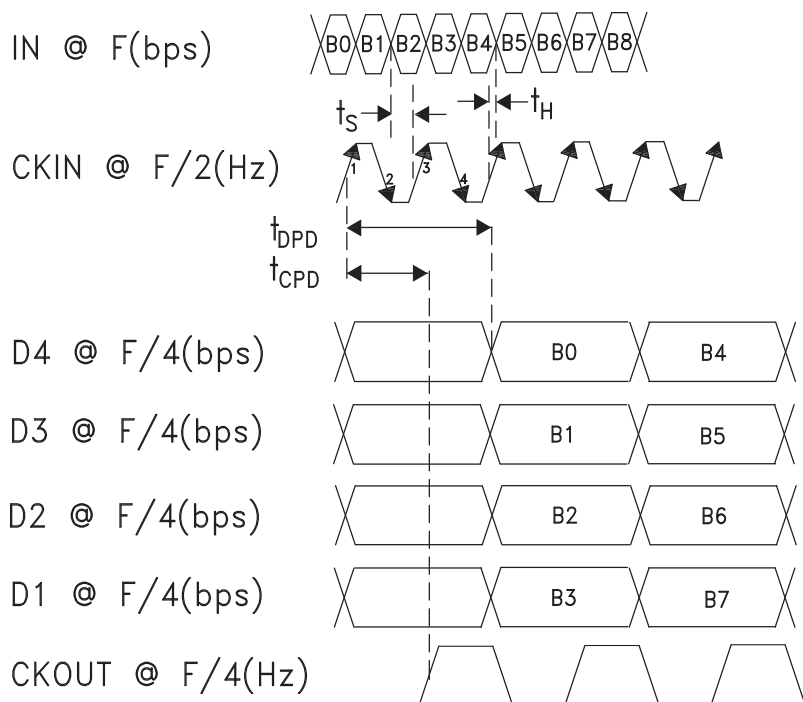
INP: 40 Gbps NRZ PRBS 2<sup>23</sup>-1 pattern, 250 mVp-p single-ended

CKINP: 20 GHz Clock Signal, 250 mVp-p single-ended

[1] Vctrl = 2.5V

[2] Device measured on evaluation board with single ended time domain gating

### Timing Diagram



### Absolute Maximum Ratings

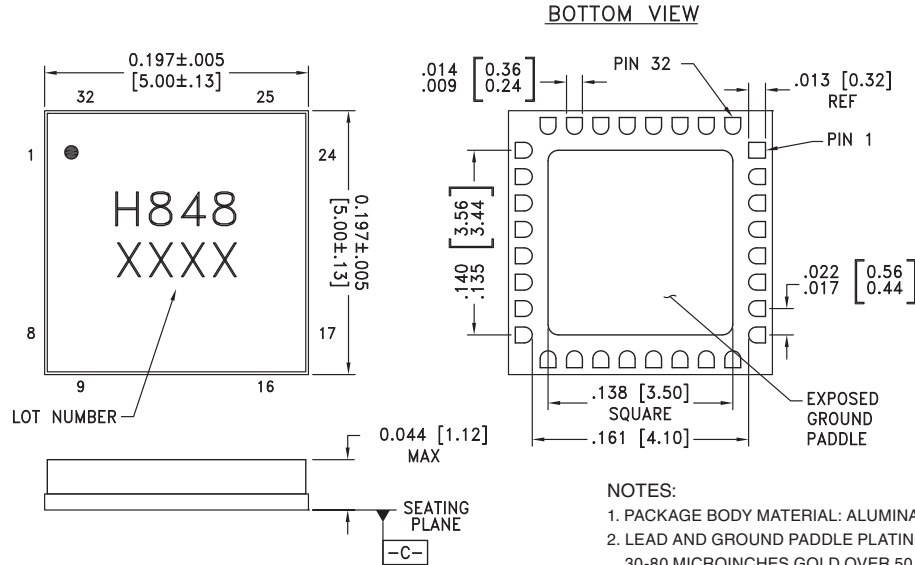
|   |                        |
|---|------------------------|
| Power Supply Voltage (Vcc)  | 3.7V to +0.5V          |
| Input Voltages  | Vcc -2V to Vcc +0.5V   |
| DC Control Pins (Vctrl, Vdccc)                                    | Vcc +0.2V to Vcc -2.5V |
| Channel Temperature   | 125 °C                 |
| Continuous Pdiss (T = 85 °C)<br>(derate 49.97 mW/°C above 85 °C ) | 2 W                    |
| Thermal Resistance<br>(Channel to die bottom)                     | 20.01 °C/W             |
| Storage Temperature   | -65°C to +150°C        |
| Operating Temperature   | -40°C to +85°C         |



ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS

## 45 Gbps, 1:4 DEMUX WITH PROGRAMMABLE OUTPUT VOLTAGE

### Outline Drawing

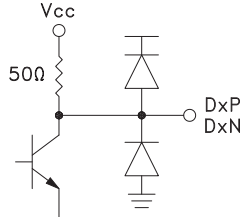

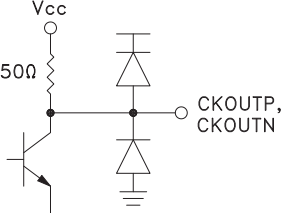
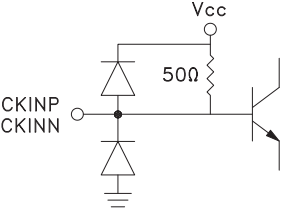
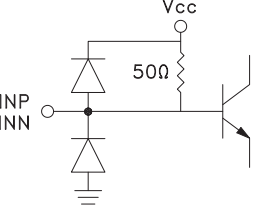
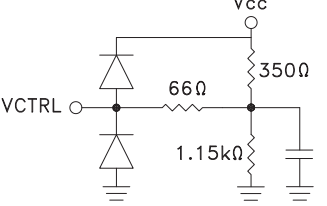


#### NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:  
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO V<sub>ee</sub>.

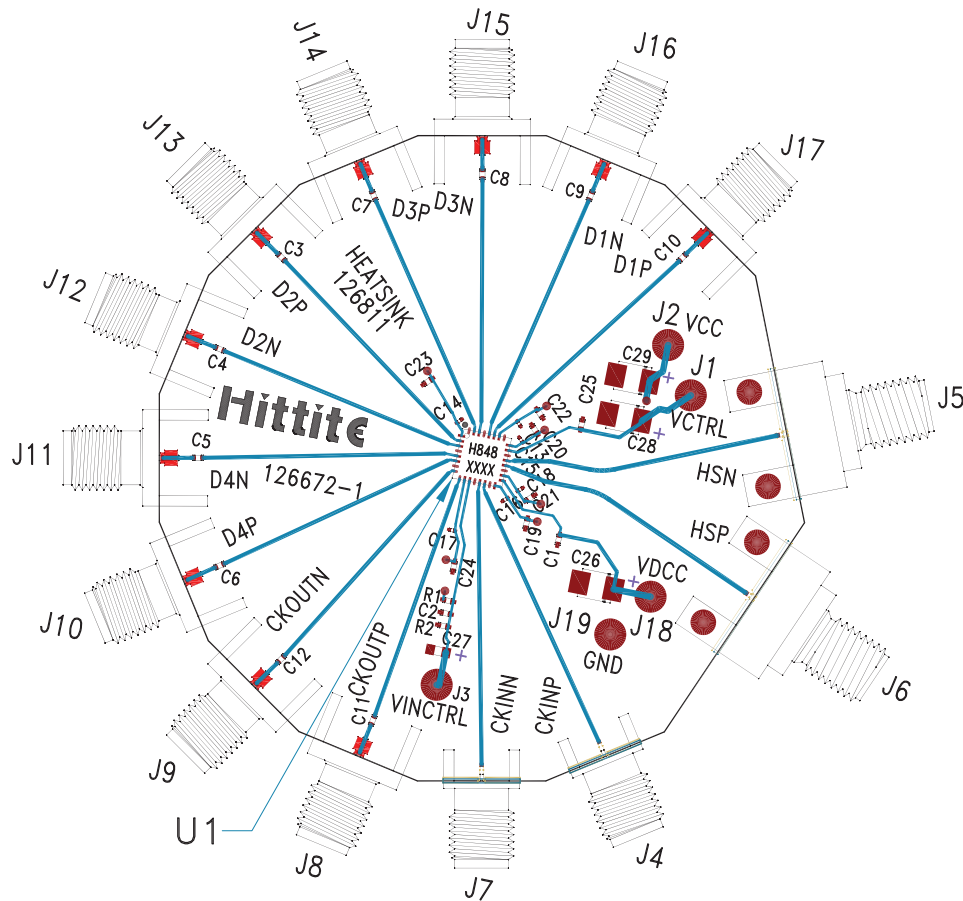
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**Pin Descriptions**

| Pin Number                          | Function                                     | Description                                     | Interface Schematic   |
|-------------------------------------|--|---|---|
| 1, 10, 16,<br>24, 26                | VCC  | Positive supply (3.3V)                          |   |
| 2, 3, 5, 6, 27,<br>28, 30, 31       | D2P, D2N, D4N,<br>D4P, D1P, D1N,<br>D3N, D3P | Differential 4 Channel Serial Data Outputs      |    |
| 4, 7, 12, 15, 19,<br>22, 25, 29, 32 | GND  | Signal and supply ground.                       |    |
| 8, 9                                | CKOUTN,<br>CKOUTP                            | Differential Quarter Rate System Clock Outputs. |   |
| 11, 17, 18                          | N/C  | Not connected.                                  |   |
| 13, 14                              | CKINN, CKINP                                 | Differential Half Rate Clock Inputs.            |  |
| 20, 21                              | INP, INN                                     | High Speed Serial Data Inputs                   |  |
| 23                                  | Vctrl  | Output Amplitude Control                        |  |

## 45 Gbps, 1:4 DEMUX WITH PROGRAMMABLE OUTPUT VOLTAGE

### Evaluation PCB



### List of Materials for Evaluation PCB 126674 [1]

| Item             | Description                 |
|------------------|-----------------------------|
| J1, J2, J18, J19 | DC Connector                |
| J4, J7           | K Connector                 |
| J5, J6           | 2.4mm Connector             |
| J8 - J17         | SMA Connector               |
| C1, C19 - C25    | 100 nF Capacitor, 0402 Pkg. |
| C3 - C12         | 10 nF Capacitor, 0402 Pkg.  |
| C13 - C18        | 1 nF Capacitor, 0201 Pkg.   |
| C26, C28, C29    | 4.7 µF Capacitor, Tantalum  |
| U1               | HMC848LC5 45 Gbps 1:4 Demux |
| PCB [2]          | 126672 Evaluation Board     |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

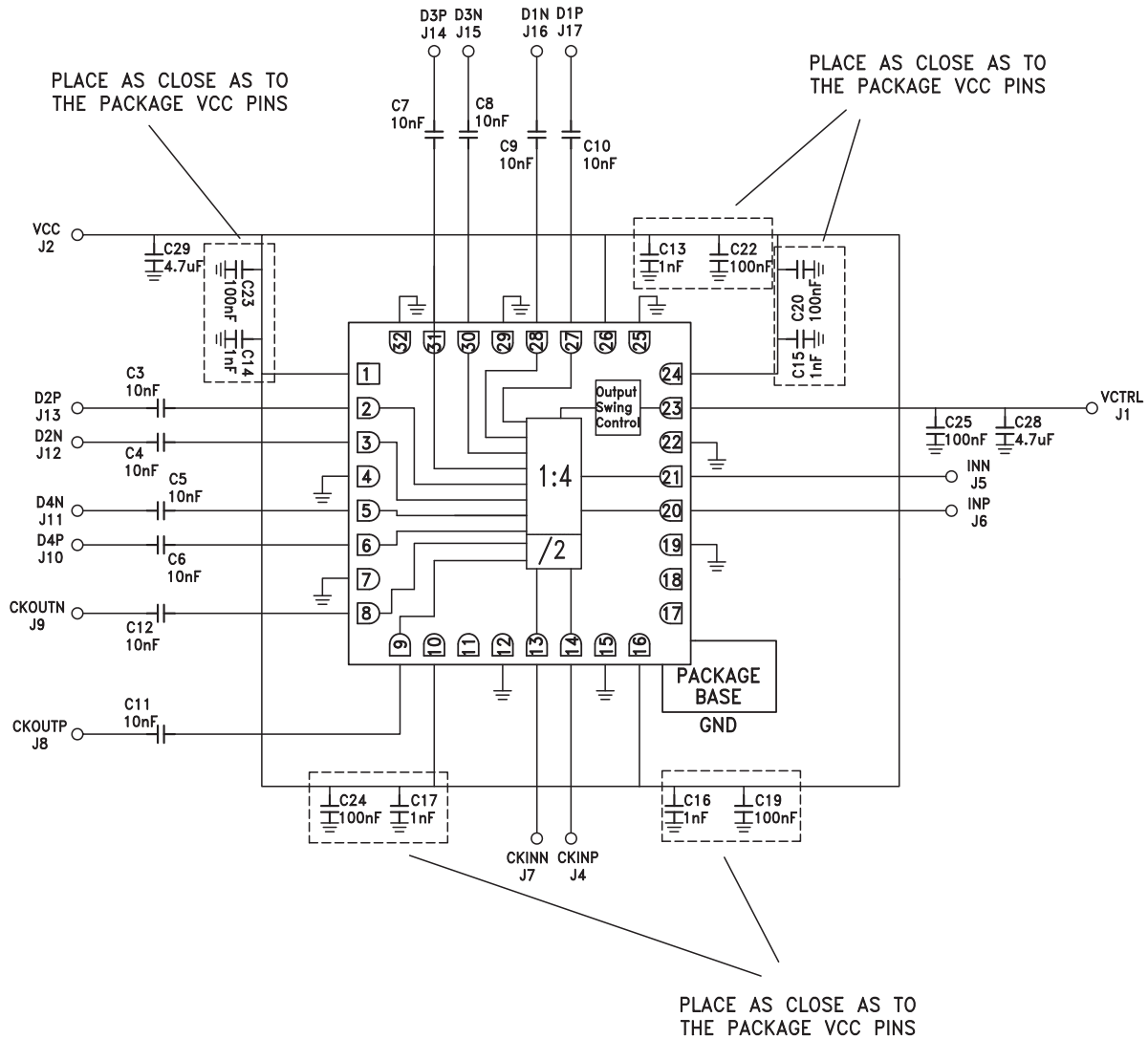
The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.





**45 Gbps, 1:4 DEMUX WITH  
PROGRAMMABLE OUTPUT VOLTAGE**

**Application Circuit**





MICROWAVE CORPORATION v01.1010



**HMC848LC5**

**45 Gbps, 1:4 DEMUX WITH  
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**Notes:**

**3**

**MUX & DEMUX - SMT**