RoHS Compliant

Value Added Compact Flash Series Ⅲ

Datasheet for Industrial CF

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Version 1.6

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Features:

- **Compact Flash Association Specification Revision 3.0 Standard Interface**
  - ATA command set compatible
  - ATA mode support for up to:
    PIO Mode-6
    Multiword DMA Mode-4
    Ultra DMA Mode-4
- **Connector Type**
  - 50 pins female
- **Low power consumption (typical)**
  - Supply voltage: 3.3V & 5V
  - Active mode: 80 mA/95 mA (3.3V/5.0V)
  - Sleep mode: 700 µA/900 µA (3.3V/5.0V)
- **Performance**
  - Sustained read: up to 35 MB/sec
  - Sustained write:
    Standard: up to 15 MB/sec
    High Speed: up to 25 MB/sec
- **Capacity**
  - Standard:
    128, 256, 512 MB
    1, 2, 16 GB
  - High Speed:
    256, 512 MB
    1, 2, 4, 8 GB
- **NAND Flash Type: SLC**
- **Temperature ranges**
  - Operation:
    Standard: 0℃ to 70℃
    ET[1]: -40℃ to 85℃
  - Storage: -40℃ to 100℃
- **Flash management**
  - Intelligent endurance design
    Advanced wear-leveling algorithms
    S.M.A.R.T. technology
    Built-in hardware ECC
    Enhanced data integrity
  - Intelligent power failure recovery
- **RoHS compliant**

1. Extended Temperature

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1. General Description

Apacer's Industrial Compact Flash Card (CFC) offers the most reliable and high performance storage which is compatible with CF Type I and Type II devise. Unlike the ordinary consumer Compact Flash cards, Apacer Industrial Compact Flash card provides solid traceability to ensure all products HW/SW are the same as you qualified.

Apacer's CFC provides complete PCMCIA - ATA functionality and compatibility. Apacer 's Compact Flash technology is designed for use in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications.

Featuring technologies as Advanced Wear-leveling algorithms, S.M.A.R.T, Enhanced Data Integrity, Built-in Hardware ECC, and Intelligent Power Failure Recovery, Apacer's Industrial Compact Flash Card assures users of a versatile device on data storage.

1.1 Performance-Optimized Controller

The Compact Flash Card Controller translates standard CF signals into flash media data and control signals.

1.1.1 Power Management Unit (PMU)

The power management unit (PMU) controls the power consumption of the Compact Flash card controller. It reduces the power consumption of the Compact Flash Card Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

1.1.2 SRAM Buffer

The Compact Flash Card Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

2. Functional Block

The Compact Flash Card (CFC) includes a controller and flash media, as well as the Compact Flash standard interface. Figure 2-1 shows the functional block diagram.

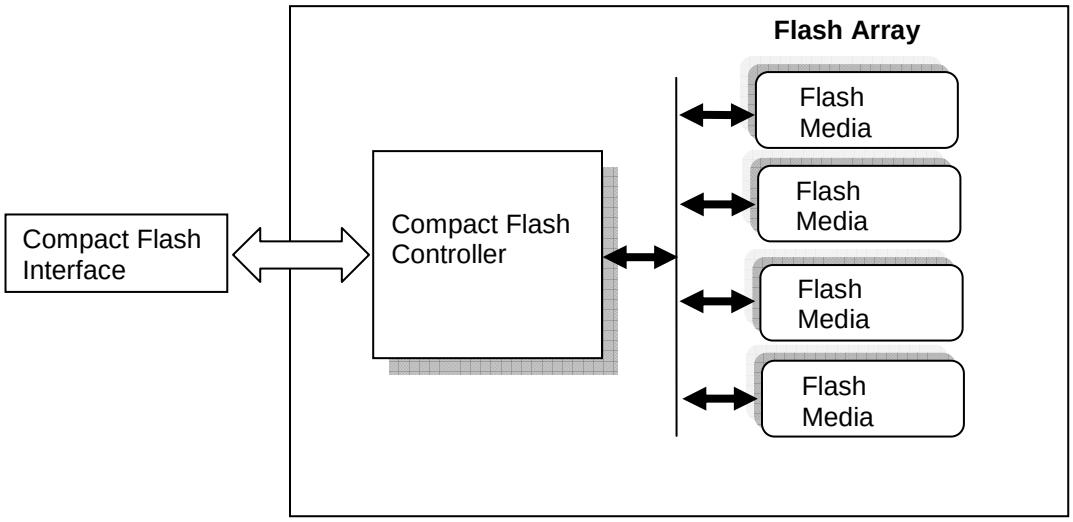


Figure 2-1: Functional block diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A "#" suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1: Pin assignments (1 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CS0	I
8	A10	I	A10	I	A10[1]	I
9	#OE	I	#OE	I	#ATA SEL	I
10	A9	I	A9	I	A9[1]	I
11	A8	I	A8	I	A8[1]	I
12	A7	I	A7	I	A7[1]	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6[1]	I
15	A5	I	A5	I	A5[1]	I
16	A4	I	A4	I	A4[1]	I
17	A3	I	A3	I	A3[1]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOIS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	#CE2	I	#CE2	I	#CS1	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	#IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	#RESET	I

Table 3-1: Pin assignments (2 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ[2]	O
44	#REG	I	#REG	I	DMACK[2]	I
45	BVD2	O	#SPKR	O	#DASP	O
46	BVD1	O	#STSCHG	O	#PDIAG	O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

1. The signal should be grounded by the host.
2. Connection required when UDMA is in use.

4. Capacity Specification

Capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity specifications

Capacity	Total bytes[1,2]	Cylinders	Heads	Sectors	Max LBA
128 MB	128,450,560	980	8	32	250,880
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1GB	1,024,966,656	1,986	16	63	2,001,888
2GB	2,048,901,120	3,970	16	63	4,001,760
4GB	4,110,188,544	7,964	16	63	8,027,712
8GB	8,195,604,480	15,880	16	63	16,007,040
16GB	16,391,208,960	16,383[3]	16	63	32,014,080

1. Total bytes includes system block.
2. Display of total bytes varies from operating systems.
3. Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

4.1 Performance Specification

Performances of the Standard and High Speed ATA-Flash Disk are listed in Table 4-2 and Table 4-3.

Table 4-2: Standard Performance specifications

Capacity / Performance	128 MB / 256 MB 512 MB / 1 GB	2 GB	16 GB
Sustained read (MB/s)	19	35	22
Sustained write (MB/s)	7	15	15

Table 4-3: High Speed Performance specifications

Capacity / Performance	256 MB / 512 MB	1GB / 2 GB / 4 GB / 8 GB
Sustained read (MB/s)	30	35
Sustained write (MB/s)	13	22~25

4.2 Environmental Specifications

Environmental specification of the Compact Flash Card series (CFC) which follows the MIL-STD-810F standards is available as shown in Table 4-4.

Table 4-4: Environmental specifications

Environment		Specification
Temperature	Operation	0℃ to 70℃; -40℃ to 85℃ (ET [1])
	Storage	-40℃ to 100℃
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operation)		Sine wave: 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes)

1. Extended Temperature

5. Flash Management

5.1 Intelligent Endurance Design

5.1.1 Advanced wear-leveling algorithms

The NAND flash devices are limited by a certain number of write cycles. When using a file system, frequent file table updates is mandatory. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole device, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. The scheme is achieved both via buffer management and Apacer-specific advanced wear leveling to ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

5.1.2 S.M.A.R.T. Technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

5.1.3 Built-in Hardware ECC

The ATA-Disk Module uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data. High performance is fulfilled through hardware-based error detection and correction.

5.1.4 Enhanced Data Integrity

The properties of NAND flash memory make it ideal for applications that require high integrity while operating in challenging environments. The integrity of data to NAND flash memory is generally maintained through ECC algorithms and bad block management. Flash controllers can support up to 8 bits ECC capability for accuracy of data transactions, and bad block management is a preventive mechanism from loss of data by retiring unusable media blocks and relocating the data to the other blocks, along with the integration of advanced wear leveling algorithms, so that the lifespan of device can be expanded.

5.2 Intelligent Power Failure Recovery

The Low Power Detection on the controller initiates cached data saving before the power supply to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected blackout. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

6. Software Interface

6.1 Command Set

Table 6-1 summarizes the command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1: Command set (1 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
Flush-Cache	E7H	-	-	-	-	D	-
Format Track	50H	-	Y[7]	-	Y	Y[8]	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Request-Sense	03H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y[7]	-	-	-	D	-

Table 6-1: Command set (2 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
SMART	B0H	Y	Y	Y	Y	D	
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Translate-Sector	87H	-	Y	Y	Y	Y	Y
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-Without-Erase	CDH	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector-Without-Erase	38H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address mode supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command
8. For the Drive/Head register:
Y means both the CFC and Head parameters are used
D means only the CFC parameter is valid and not the Head parameter

6.1.1 Check-Power-Mode – E5H or 98H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E5H or 98H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode. Because the compact flash card can recover from sleep in 200 ns, idle mode is never enabled. The compact flash card sets BSY, sets the Sector Count register to 00H, clears BSY and generates an interrupt.

6.1.2 Execute-Drive-Diagnostic – 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the compact flash card. If the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices, the Diagnostic codes shown in Table 6-2 are returned in the Error register at the end of the command.

Table 6-2: Diagnostic codes

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error

6.1.3 Erase-Sector(s) – C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (4)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is used to pre-erase and condition data sectors in advance of a Write-Without-Erase or Write-Multiple-Without-Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

6.1.4 Flush-Cache – E7H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the compact flash card to complete writing data from its cache. The compact flash card then clears BSY and generates an interrupt.

6.1.5 Format-Track – 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (4)	X (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is accepted for host backward compatibility. The compact flash card expects a sector buffer of data from the host to follow the command with the same protocol as the Write-Sector(s) command although the compact flash card does not use the information in the buffer. The use of this command is not recommended.

6.1.6 Identify-Drive – ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the compact flash card. This command has the same protocol as the Read- Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 6-3. All reserved bits or words are zero. Table 6-3 is the definition for each field in the Identify-Drive Information.

Table 6-3: Identify-Drive information (1 of 3)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit-significant information

Table 6-3: Identify-Drive information (2 of 3)

Word Address	Default Value	Total Bytes	Data Field Type Information
1	bbbbH[2]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[2]	2	Default number of heads
4	0000H	2	Reserved
5	0200H	2	Reserved
6	bbbbH[2]	2	Default number of sectors per track
7-8	bbbbH[2]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-19	ddddH[4]	20	Unique serial number in ASCII
20	0002H	2	Buffer type
21	xxxxH	2	Vendor Unique
22	xxxxH	2	Vendor Unique
23-26	aaaaH[5]	8	Firmware revision in ASCII.
27-46	ccccH[6]	40	Definable Model number/name
47	8001H	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0007H	2	Translation parameters are valid
54	nnnnH[3]	2	Current numbers of cylinders
55	nnnnH[3]	2	Current numbers of heads
56	nnnnH[3]	2	Current sectors per track
57-58	nnnnH[3]	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010X	2	Multiple sector setting
60-61	nnnnH[3]	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Reserved
63	0x07H	2	DMA data transfer is supported in the compact flash card.
64	0003H	2	Advanced PIO Transfer Mode supported
65	0078H	2	120 ns cycle time support for Multiword DMA Mode-2
66	0078H	2	120 ns cycle time support for Multiword DMA Mode-2
67	0078H	2	PIO Mode-4 supported

Table 6-3: Identify-Drive information (3 of 3)

Word Address	Default Value	Total Bytes	Data Field Type Information
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80	007EH	2	ATA/ATAPI major version number
81	0019H	2	ATA/ATAPI minor version number
82	706BH	2	Features/command sets supported
83	400CH	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88	xx1FH	2	UDMA mode
89	xxxxH	2	Time required for security erase unit completion
90	xxxxH	2	Time required for enhanced security erase unit completion
91-127	0000H	72	Reserved
128	xxxxH	2	Security Status
129-159	0000H	62	Vendor unique bytes
160-162	000H	6	Reserved
163	xx2H	2	Reserved
164-255	0000H	190	Reserved

1. XXXX=This field is subject to change by the host or the device
2. bbbb - default value set by controller. The selections could be user programmable.
3. n - calculated data based on product configuration
4. dddd - unique number of each device
5. aaaa - any unique firmware revision
6. cccc - default value is “xxxMB compact flash card” where xxx is the flash drive capacity.
   The user has an option to change the model number during manufacturing.

- **Word 0: General Configuration**

  This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MB/sec and is not MFM encoded.

- **Word 1: Default Number of Cylinders**

  This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

- **Word 3: Default Number of Heads**

  This field contains the number of translated heads in the default translation mode.

- **Word 6: Default Number of Sectors per Track**

  This field contains the number of sectors per track in the default translation mode.

- **Word 7-8: Number of Sectors**

  This field contains the number of sectors per compact flash card. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

- **Word 10-19: Serial Number**

  Unique serial number ID. The twenty bytes are a user-programmable value with a default value of spaces.

- **Word 20: Buffer Type**

  This field defines the buffer capability:
  0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the compact flash card.

- **Word 23-26: Firmware Revision**

  This field contains the revision of the firmware for this product.

- **Word 27-46: Model Number**

  This field contains the model number for this product.

- **Word 47: Read-/Write-Multiple Sector Count**

  This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only a value of '1' is supported.

- **Word 49: Capabilities**

Bit	Function
13	Standby Timer
	0: forces sleep mode when host is inactive.
11	IORDY Support
	1: PIO Mode-4 is supported.
9	LBA Support
	1: LBA mode addressing is supported.
8	DMA Support
	1: DMA mode is supported.

- **Word 51: PIO Data Transfer Cycle Timing Mode**

  This field defines the mode for PIO data transfer. The compact flash card module supports up to PIO Mode-

- **Word 53: Translation Parameters Valid**

Bit	Function
0	1: Words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: Words 64-70 are valid to support PIO Mode-3 and 4.
2	1: Word 88 is valid to support Ultra DMA data transfer.

- **Word 54-56: Current Number of Cylinders, Heads, Sectors/Track**

  These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

- **Word 57-58: Current Capacity**

  This field contains the product of the current cylinders times heads times sectors.

- **Word 59: Multiple Sector Setting**

  This field contains a validity flag in the Odd Byte and the current numbers of sectors that can be transferred per interrupt for R/W Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

  The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid.

- **Word 60-61: Total Sectors Addressable in LBA Mode**

  This field contains the number of sectors addressable for the compact flash card in LBA mode only.

- **Word 63: Multiword DMA Transfer**

  This field identifies the Multiword DMA transfer modes supported by the compact flash card module and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time.

Bit	Function
15-11	Reserved
10	Multiword DMA mode-2 selected 1: Multiword DMA mode-2 is selected and bits 8 and 9 are cleared to 0. 0: Multiword DMA mode-2 is not selected.
9	Multiword DMA mode-1 selected 1: Multiword DMA mode-1 is selected and 8 and 10 shall be cleared to 0. 0: Multiword DMA mode-1 is not selected.
8	Multiword DMA mode-0 selected 1: Multiword DMA mode-0 is selected and bits 9 and 10 are cleared to 0. 0 then Multiword DMA mode-0 is not selected.
7-3	Reserved
2	Multiword DMA mode-2 supported 1: Multiword DMA mode-2 and below are supported and Bits 0 and 1 shall be set to 1.
1	Multiword DMA mode-1 supported 1: Multiword DMA mode-1 and below are supported.
0	Multiword DMA mode-0 supported 1: Multiword DMA mode-0 is supported.

- **Word 64: Advanced PIO Data Transfer Mode**

  Bit (7:0) is defined as the PIO data and register transfer supported field. If this field is supported, Bit 1of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bit (7:2) are Reserved for future PIO modes.

Bit	Function
0	1: PIO Mode-3 is supported.
1	1: PIO Mode-4 is supported.

- **Word 65: Minimum Multiword DMA Transfer Cycle Time Per Word**

  This field defines the minimum Multiword DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the compact flash card supports when performing Multiword DMA transfers on a per word basis. The compact flash card supports up to Multiword DMA Mode-2, so this field is set to 120ns.

- **Word 66: Device Recommended Multiword DMA Cycle Time**

  This field defines the compact flash card recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the compact flash card may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. The compact flash card supports up to Multiword DMA Mode-2, so this field is set to 120ns.

- **Word 67: Minimum PIO Transfer Cycle Time Without Flow Control**

  This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The compact flash card minimum cycle time is 120 ns. A value of 0078H is reported.

- **Word 68: Minimum PIO Transfer Cycle Time with IORDY**

  This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfer while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The compact flash card minimum cycle time is 120 ns, e.g., PIO mode 4. A value of 0078H is reported.

- **Word 80: Major Version Number**

  If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits (6:1) being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. The compact flash card supports ATA-1 to ATA-6.

- **Word 81: Minor Version Number**

  If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 shall be 0000H or FFFFH.

  A value of 0019H reported in word 81 indicates ATA/ATAPI-6 T13 1410D revision 3a guided the implementation.

- **Words 82-84: Features/command sets supported**

  Words 82, 83, and 84 indicate the features and command sets supported.

  Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	1: Security Mode feature set is supported
0	0: SMART feature set is not supported

  Word 83

  The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are not valid
14	1: Provides indications that the features/command sets supported words are valid
13-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is not supported
2	1: CFA feature set is not supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	1: Download Microcode command is not supported

  Word 84

  The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are valid
14	1: Provides indications that the features/command sets supported words are valid
13-0	0: Reserved

- **Words 85-87: Features/command sets enabled**

  Words 85, 86, and 87 indicate features/command sets enabled. The host can enable/disable the features or command set only if they are supported in Words 82-84.

  Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0: Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	1: Host Protected Area feature set is not enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled
1	0: Security Mode feature set has not been enabled via the Security Set Password command 1: Security Mode feature set has been enabled via the Security Set Password command
0	0: SMART feature set is not enabled

  Word 86

Bit	Function
15-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled via the Set Features command 1: Advanced Power Management feature set is enabled via the Set Features command
2	0: CFA feature set is disenabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

  Word 87

  The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are valid
14	1: Provides indications that the features/command sets supported words are valid
13-0	0: Reserved

Word 88

Bit	Function
15-13	Reserved
12	1: Ultra DMA mode-4 is selected 0: Ultra DMA mode-4 is not selected
11	1: Ultra DMA mode-3 is selected 0: Ultra DMA mode-3 is not selected
10	1: Ultra DMA mode-2 is selected 0: Ultra DMA mode-2 is not selected
9	1: Ultra DMA mode-1 is selected 0: Ultra DMA mode-1 is not selected
8	1: Ultra DMA mode-0 is selected 0: Ultra DMA mode-0 is not selected
7-5	Reserved
4	1: Ultra DMA mode-4 and below are supported
3	1: Ultra DMA mode-3 and below are supported
2	1: Ultra DMA mode-2 and below are supported
1	1: Ultra DMA mode-1 and below are supported
0	1: Ultra DMA mode-0 is supported

- **Word 89: Time required for Security erase unit completion**

  Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

- **Word 90: Time required for Enhanced security erase unit completion**

  Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

- **Word 128: Security Status**

Bit	Function
8	Security Level 1: Security mode is enabled and the security level is the maximum 0: and security mode is enabled, indicates that the security level is high
5	Enhanced security erase unit feature supported 1: Enhanced security erase unit feature set is supported
4	Expire 1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset
3	Freeze 1: Security is frozen
2	Lock 1: Security is locked

1 Enable/Disable
1: Security is enabled
0: Security is disabled
0 Capability
1: supports security mode feature set
0: does not support security mode feature set

6.1.7 Idle – E3H or 97H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E3H or 97H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5msec increments)							
Feature (1)	X							

This command causes the compact flash card to set BSY, enter the Idle Mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero and the automatic power down mode is also enabled, the timer count is set to 3, with each count being 5ms. Note that this time base (5msec) is different from the ATA specification.

6.1.8 Idle-Immediate – E1H or 95H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E1H or 95H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the compact flash card to set BSY, enter the Idle Mode, clear BSY and generate an interrupt.

6.1.9 Initialize-Drive-Parameters – 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

6.1.10 NOP – 00H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	00H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command always fails with the compact flash card returning command aborted.

6.1.11 Read-Buffer – E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Buffer command enables the host to read the current contents of the compact flash card's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.1.12 Read DMA – C8H or C9H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8H or C9H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to the READ SECTOR (S) command except for the following:

- The host initializes the DMA channel prior to issuing the command;
- Data transfers are qualified by DMARQ and are performed by the DMA channel;
- The compact flash card issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a READ DMA command, the compact flash card shall provide status of the BSY bit or the DRQ bit until the command is completed. At command completion, the command block registers contain the cylinder, head and sector number (LBA) of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The flawed data is pending in the sector buffer. Subsequent sectors are transferred only if the error was a correctable data error. All other errors cause Read-DMA to stop after transfer of the sector that contained the error.

For Ultra-DMA mode, if a CRC error is detected during transfer, the ICRC and ABRT bits of the Error register are set at the end of the command.

6.1.13 Read-Multiple – C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The Read- Multiple command is similar to the Read- Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set-Multiple command.

Command execution is identical to the Read- Sectors operation except that the numbers of sectors defined by a Set-Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple Mode command, which must be executed prior to the Read- Multiple command. When the Read-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer.

The partial block transfer is for n sectors, where n = remainder (sector count/block count). If the Read-Multiple command is attempted before the Set-Multiple Mode command has been executed or when Read-Multiple commands are disabled, the Read-Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read- Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read-Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector counts of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

6.1.14 Read Sectors – 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sectors count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the compact flash card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

6.1.15 Read Verify Sector(s) – 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read- Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the compact flash card sets BSY.

When the requested sectors have been verified, the compact flash card clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Verify terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count register contains the number of sectors not yet verified.

6.1.16 Recalibrate – 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	X	LBA	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a no operation command to the compact flash card and is provided for compatibility purposes.

6.1.17 Request-sense – 03H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests extended error information for the previous command. Table 6-4 defines the valid extended error codes for the compact flash card. The extended error code is returned to the host in the Error register.

Table 6-4: Extended Error Codes

Extended Error Code	Description
00H	No Error Detected
01H	Self Test OK (No Error)
09H	Miscellaneous Error
20H	Invalid Command
21H	Invalid Address (Requested Head or Sector Invalid)
2FH	Address Overflow (Address Too Large)
35H, 36H	Supply or generated Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Corrected ECC Error
05H, 30-34H, 37H, 3EH	Self Test or Diagnostic Failed
10H, 14H	ID Not Found
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media f Format
03H	Write / Erase Failed
22H	Power Level 1 Disabled

6.1.18 Seek – 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the compact flash card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.1.19 Set-Features – EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 6-5 defines all features that are supported.

Table 6-5: Features supported

Feature	Operation
01H	Enable 8-bit data transfers.
02H	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 4-9 defines the values.
09H	Enable Extended Power Operations
55H	Disable Read Look Ahead.
66H	Disable Power- on Reset (POR) establishment of defaults at software Reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H	Disable Write Cache
89H	Disable Extended Power operations
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
AAH	Enable Read Look Ahead.
CCH	Enable Power- on Reset (POR) establishment of defaults at software Reset.

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the compact flash card that implements write cache. When the subcommand Disable-Write-Cache is issued, the compact flash card should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 55H is the default feature for the compact flash card. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

Table 6-6: Transfer mode values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multiword DMA mode	00100b	mode[1]
Ultra-DMA mode	01000b	mode[1]
Reserved	Other	N/A

1. Mode = transfer mode number, all other values are not valid

6.1.20 SMART – B0H

Smart Command signature is defined as cylinder being C2H to F4H. The feature register will indicate the subcommand as listed below.

- **6.1.20.1 SMART Return Status – DAH**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	DAH							

This Command is used to communicate the reliability status of the device to the host at the host's request. If the device has not detected a threshold exceeded condition, the device sets the LBA Mid register to 4FH and the LBA High register to C2H. If the device has detected a threshold exceeded condition, the device sets the LBA Mid register to F4H and the LBA High register to 2CH. In the current implementation, the only threshold checked is that a fatal error has occurred.

- **6.1.20.2 SMART Enable/Disable Attribute Autosave – D2H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	00H or F1H							
Feature (1)	D2H							

This Command enables or disables the optional attribute autosave feature of the device. A value of 00H in the Sec Cnt register will disable the autosave feature. A value of F1H in the Sec Cnt register will enable the autosave feature. Currently, no action is generated by this command since there in no online collection of data.

- **6.1.20.3 SMART Enable Operations – D8H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D8H							

This Command enables access to all SMART capabilities within the device. Prior to receipt of this command, SMART data is collected but not accessible via SMART. The state of SMART (either enabled or disable) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

- **6.1.20.4 SMART Disable Operations – D9H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D9H							

This Command disables access to SMART data via SMART commands. After receipt of this command the device shall disable all SMART operations. However SMART data shall continue to be collected and accessible when SMART is next enabled. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. After receipt of this command by the device, all other SMART commands, including SMART DISABLE OPERATIONS commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid, and the commands shall aborted by the device.

- **6.1.20.5 SMART Execute Offline – D4H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	Subcommand Specific							
Sec Cnt (2)	X							
Feature (1)	DAH							

This Command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and the save this data to the device's memory. This data is not retained across resets and a new command must be executed to recollect data. The SMART data collected is determined by the subcommand specified in the Sec Num register. All subcommands other than listed below will be aborted. Valid subcommands will be executed in captive mode and the device will set BSY bit until command is completed. The collected data should be read by a subsequent SMART Read Data (D0H) command.

SMART EXECUTE OFF-LINE Sector Number register values (sub-command specific)

Subcommand	Collected Data
0-201	Reserved
202 (0xCA)	Bad block count (captive)
203 (0xCB)	Group free block count (captive)
204 (0xCC)	Group average age (captive)
205 (0xCD)	Group maximum age (captive)
206 (0xCE)	Group minimum age (captive)
207 (0xCF)	Group wear swap count (captive)
208 (0xD0)	Group retention swap count (captive)
209 (0xD1)	Group total block erase count (captive)
210-255	Reserved

- **6.1.20.6 SMART Read Data – D0H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D0H							

This Command returns the Device SMART data structure to the host. This command must be preceded by the SMART Execute Offline command with an appropriate subcommand listed above. The returned data will depend on the requested subcommand.

All returned data comply with the SMART data structure as specified in the ATA spec. Bytes 0 to 361 of the structure returns SST specific data that depends of the requested subcommand. Bytes 362 to 385 are standard values as defined in the ATA spec. bytes 386 to 510 returns SST specific data common to all subcommands. Byte 511 is the 2's complement checksum of all bytes in the data structure.

Offline Data Collection Status (byte 362)

The offline data collection status byte indicates whether SMART data collection was successful or not. The host should check this value in the returned data structure before proceeding with interpretation of vendor specific data bytes. The follow are possible status values.

Value	Definition
00H	Offline data collection activity was never started.
02H	Offline data collection activity was completed without error.
04H	Offline data collection activity was suspended host.
05H	Offline data collection activity was aborted by host.
06H	Offline data collection activity was aborted by device.

6.1.21 Set-Multiple-Mode – C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the compact flash card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count register is loaded with the number of sectors per block. Upon receipt of the command, the compact flash card sets BSY to 1 and checks the Sector Count register.

If the Sector Count register contains a valid value and the block count is supported, the value is loaded for all subsequent Read-Multiple and Write-Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted command error is posted, and Read- Multiple and Write- Multiple commands are disabled. If the Sector Count registers contains 0 when the command is issued, Read and Write- Multiple commands are disabled. At power-on, or after a hardware or (unless disabled by a Set-Feature command) software reset, the default mode is Read and Write-Multiple disabled.

6.1.22 Set-Sleep-Mode – E6H or 99H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E6H or 99H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the compact flash card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

6.1.23 Standby – E2H or 96H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E2H or 96H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the compact flash card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by simply issuing another command (a reset is not required).

6.1.24 Standby-Immediate – E0H or 94H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E0H or 94H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the compact flash card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by simply issuing another command (a reset is not required).

6.1.25 Translate-Sector – 87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 Byte buffer of information containing the desired cylinder, head, and sector, including its logical address, and the Hot Count, if available, for that sector. Table 6-7 represents the information in the buffer. Please note that this command is unique to the compact flash card.

Table 6-7: Translate- Sector Information

Address	Information
00H-01H	Cylinder MSB (00), Cylinder LSB (01)
02H	Head
03H	Sector
04H-06H	LBA MSB (04) - LSB (06)
07H-12H	Reserved
13H	Erased flag (FFh) = Erased; 00h = Not erased
14H-17H	Reserved
18H-1AH	Hot Count MSB (18) - LSB (1A)[1]
1BH-1FFH	Reserved

1. A value of 0 indicates Hot Count is not supported.

6.1.26 Write-Buffer – E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write-Buffer command enables the host to overwrite contents of the compact flash card sector buffer with any data pattern desired. This command has the same protocol as the Write-Sector(s) command and transfers 512 byes.

6.1.27 Write-DMA – CAH or CBH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAH or CBH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to Write-RITE Sector(s) except for the following:

- The host initializes the DMA channel prior to issuing the command

- Data transfers are qualified by DMARQ and are performed by the DMA channel

- The compact flash card issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a Write-RITE DMA command, the compact flash card shall provide status of the BSY bit or the DRQ bit until the command is completed. At command completion, the command block registers contain the cylinder, head and sector number (LBA) of the last sector read.

If an error occurs after the attempted write of a transferred sector, the command is terminated and subsequent blocks are not transferred. The command block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors for successful completion of the command.

For Ultra-DMA mode, if a CRC error is detected during transfer, the ICRC and ABRT bits of the Error register are set at the end of the command.

6.1.28 Write-Multiple – C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High (LBA23-16)							
Cyl Low (4)	Cylinder Low (LBA15-8)							
Sec Num (3)	Sector Number (LBA7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the compact flash card can support up to a block count of 1 as indicated in the Identify Drive Command information.

This command is similar to the Write-Sectors command. The compact flash card sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set-Multiple. Command execution is identical to the Write-Sectors operation except that the number of sectors defined by the Set-Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple Mode command, which must be executed prior to the Write-Multiple command.

When the Write-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly

divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where: n = remainder (sector count/block count).

If the Write-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Write-Multiple commands are disabled, the Write-Multiple operation will be rejected with an aborted command error.

Errors encountered during Write-Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count register contains 6 and the address is that of the third sector.

6.1.29 Write-Multiple-Without-Erase – CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDH							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Multiple command with the exception that an implied Erase before Write operation is not performed. The sectors should be pre-erased with the Erase-Sector(s) command before this command is issued. If the sectors are not pre-erased with the Erase-Sector(s) command, a normal Write-Multiple operation will occur.

6.1.30 Write-Sector(s) – 30H or 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-89)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is accepted, the compact flash card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host. For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The

Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

6.1.31 Write-Sector(s)-Without-Erase – 38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Sector(s) command with the exception that an implied Erase before Write operation is not performed. This command has the same protocol as the Write-Sector(s) command. The sectors should be pre-erased with the Erase-Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase-Sector(s) command, a normal Write-Sector operation will occur.

6.1.32 Write-Verify – 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write-Sector(s) command.

7. Electrical Specification

Caution: **Absolute Maximum Stress Ratings –** Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1: Operating range

Range	Ambient Temperature	3.3V	5V
Standard	0℃ to +70℃	3.135-3.465V	4.75-5.25V
Extended Temperature	-40℃ to +85℃		

Table 7-2: Absolute maximum power pin stress ratings

Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min. to 6.5V max.
Voltage on any pin except V_{DD} with respect to GND	V	-0.5V min. to VDD + 0.5V max.

Table 7-3: Recommended system power-up timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-READY}$[1]	Power-up to Ready Operation	200	1000	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	200	1000	ms

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

7.1 DC Characteristics

Table 7-4: DC Characteristics

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1} V_{IL1}	I1	Input Voltage	2.0V	 0.8V	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	μA	V_{IN}=GND to V_{DDQ} V_{DDQ}= V_{DDQ} Max
I_{U1}	I1U	Input Pull-Up Current	-110	-1	μA	V_{OUT}=GND, V_{DDQ}= V_{DDQ} Max
V_{T+2} V_{T-2}	I2	Input Voltage Schmitt Trigger	 0.8	2.0	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	μA	V_{IN}=GND to V_{DDQ} V_{DDQ}= V_{DDQ} Max
I_{U2}	I2U	Input Pull-Up Current	-110	-1	μA	V_{OUT}=GND, V_{DDQ}= V_{DDQ} Max
V_{OH1} V_{OL1}	O1	Output Voltage	2.4	 0.4	V	I_{OH1}=I_{OH1} Min I_{OL1}=I_{OL1} Max
I_{OH1}		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL1}		Output Current		4	mA	V_{DDQ}=V_{DDQ} Min
V_{OH2} V_{OL2}	O2	Output Voltage	2.4	 0.4	V	I_{OH2}=I_{OH2} Min I_{OL2}=I_{OL2} Max
I_{OH2}		Output Current	-6		mA	V_{DDQ}=3.135V-3.465V
I_{OL2}		Output Current		6	mA	V_{DDQ}=3.135V-3.465V
I_{OH2}		Output Current	-8		mA	V_{DDQ}=4.5V-5.5V
I_{OL2}		Output Current		8	mA	V_{DDQ}=4.5V-5.5V
V_{OH6} V_{OL6}	O6	Output Voltage for DASP# pin	2.4	 0.4	V	I_{OH6}=I_{OH6} Min I_{OL6}=I_{OL6} Max
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=3.135V-3.465V
I_{OL6}		Output Current for DASP# pin		8	mA	V_{DDQ}=3.135V-3.465V
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=4.5V-5.5V
I_{OL6}		Output Current for DASP# pin		12	mA	V_{DDQ}=4.5V-5.5V
$I_{DD}^{1,2}$	PWR	Power supply current (T_a = 0℃ to +70℃)		50	mA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max
$I_{DD}^{1,2}$	PWR	Power supply current (T_a= -40℃ to +85℃)		75	mA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_a = 0℃ to +70℃)		75	μA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_a = -40℃ to +85℃)		200	μA	V_{DD}=V_{DD} Max V_{DDQ}=V_{DDQ} Max

7.2 AC Characteristics

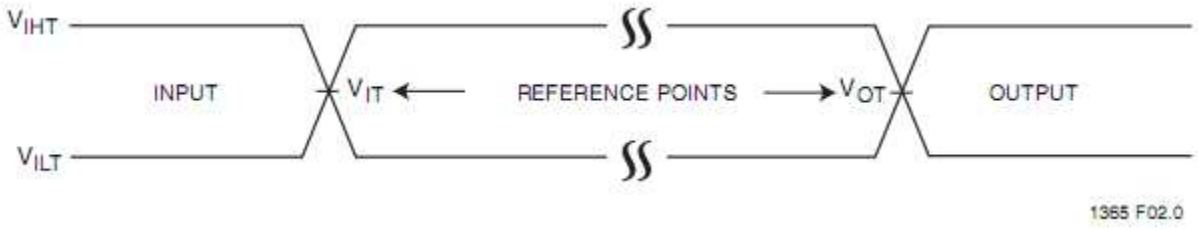


Figure 7-1: AC Input/Output Reference Waveforms

AC test inputs are driven at VIHT (0.9 VDD) for a logic "1" and VILT (0.1 VDD) for a logic "0". Measurement reference points for inputs and outputs are VIT (0.5 VDD) and VOT (0.5 VDD). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - $V_{INPUT\ HIGH}$ Test
V_{ILT}- $V_{INPUT\ LOW}$ Test

7.2.1 Attribute Memory Read Timing Specification

The Attribute Memory access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-5 Attribute Memory Read Timing Specification

Speed Version			**100 ns**		
Item	**Symbol**	**IEEE Symbol**	**Min**[1]	**Min**[1]	**Units**
Read Cycle Time	$T_{C(R)}$	tAVAV	100		ns
Address Access Time	$T_{A(A)}$	tAVQV		100	ns
Card Enable Access Time	$T_{A(CE)}$	tELQV		100	ns
Output Enable Access Time	$T_{A(OE)}$	tGLQV		50	ns
Output Disable Time from CE#	$T_{DIS(CE)}$	tEHQZ		50	ns
Output Disable Time from OE#	$T_{DIS(OE)}$	tGHQZ		50	ns
Address Setup Time	$T_{SU(A)}$	tAVGL	10		ns
Output Enable Time from CE#	$T_{EN(CE)}$	tELQNZ	5		ns
Output Enable Time from OE#	$T_{EN(OE)}$	tGLQNZ	5		ns
Data Valid from Address Change	$T_{V(A)}$	tAXQZ	0		ns

1. D_{OUT} signifies data provided by the Compact Flash card to the system. The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations. All AC specifications are guaranteed by design.

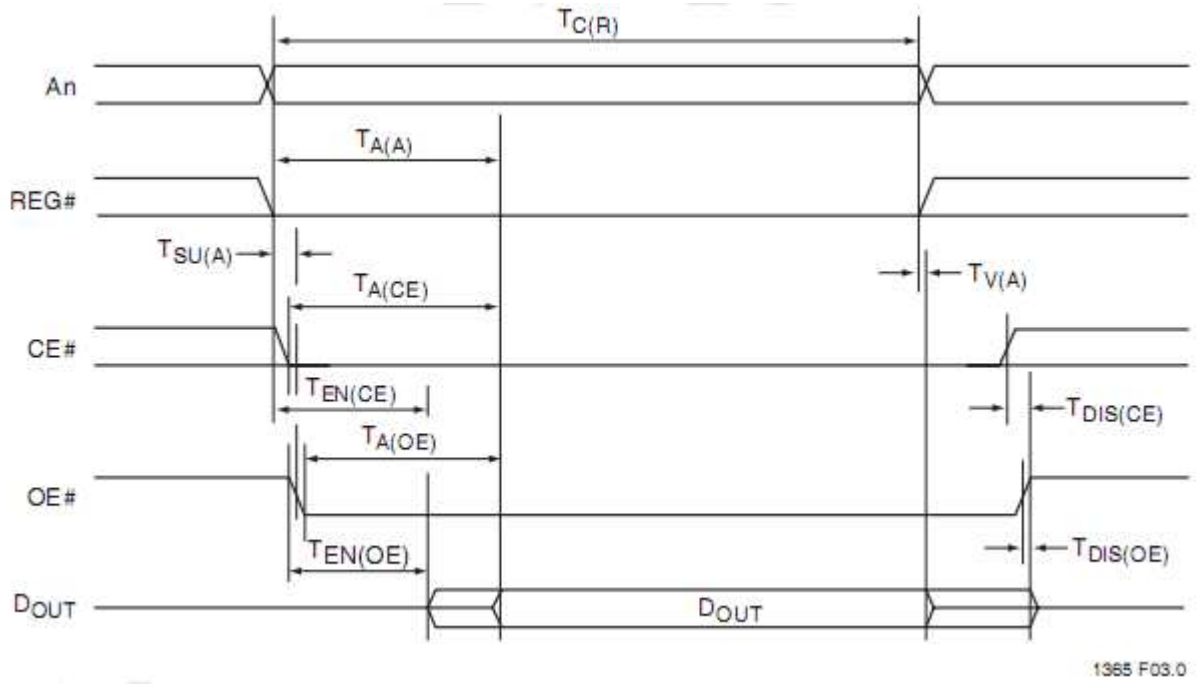


Figure 7-2: Attribute Memory Read Timing Diagram

7.2.2 Configuration Register (Attribute Memory) Write Specification

The card configuration write access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-6 Configuration Register (Attribute Memory) Write Timing

Speed Version			**100 ns**		
Item	**Symbol**	**IEEE Symbol**	**Min**[1]	**Min**[1]	**Units**
Write Cycle Time	$T_{C(W)}$	tAVAV	100		ns
Write Pulse Width	$T_{W(WE)}$	tWLWH	60		ns
Address Setup Time	$T_{SU(A)}$	tAVWL	10		ns
Write Recover Time	$T_{REC(WE)}$	tWMAX	15		ns
Data Setup Time for WE	$T_{SU(DWE\#H)}$	tDVWH	40		ns
Data Hold Time	$T_{H(D)}$	tWMDX	15		ns

1. D_{IN} signifies data provided by the system to the Compact Flash card. All AC specifications are guaranteed by design.

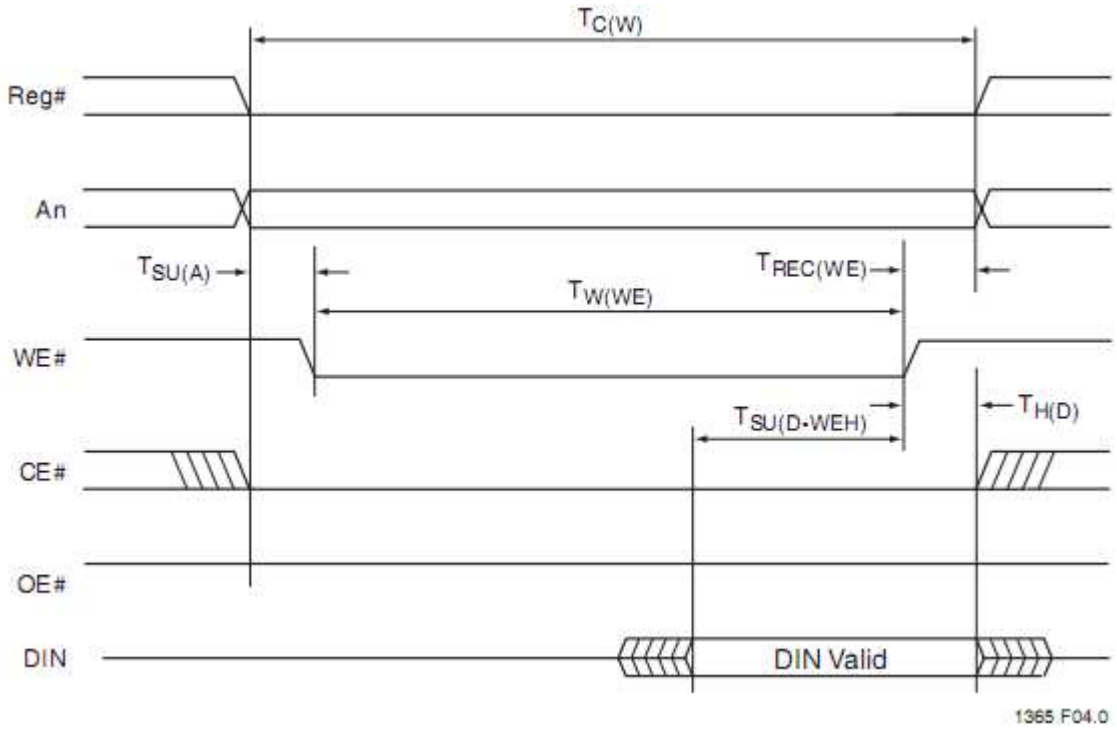


Figure 7-3: Configuration Register (Attribute Memory) Write Timing Diagram

7.2.3 Common Memory Read Timing Specification

Table 7-7 Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min[1]	Min[1]	Units
Output Enable Access Time	$T_{A(OE)}$	tGLQV		50	ns
Output Disable Time from OE	$T_{DIS(OE)}$	tGHQZ		50	ns
Address Setup Time	$T_{SU(A)}$	tAVGL	10		ns
Address Hold Time	$T_{REC(WE)}$	tGHAX	15		ns
CE Setup before OE	$T_{SU(CE)}$	tELGL	0		ns
CE Hold following OE	$T_{H(CE)}$	tGHEH	15		ns

1. All AC specifications are guaranteed by design.

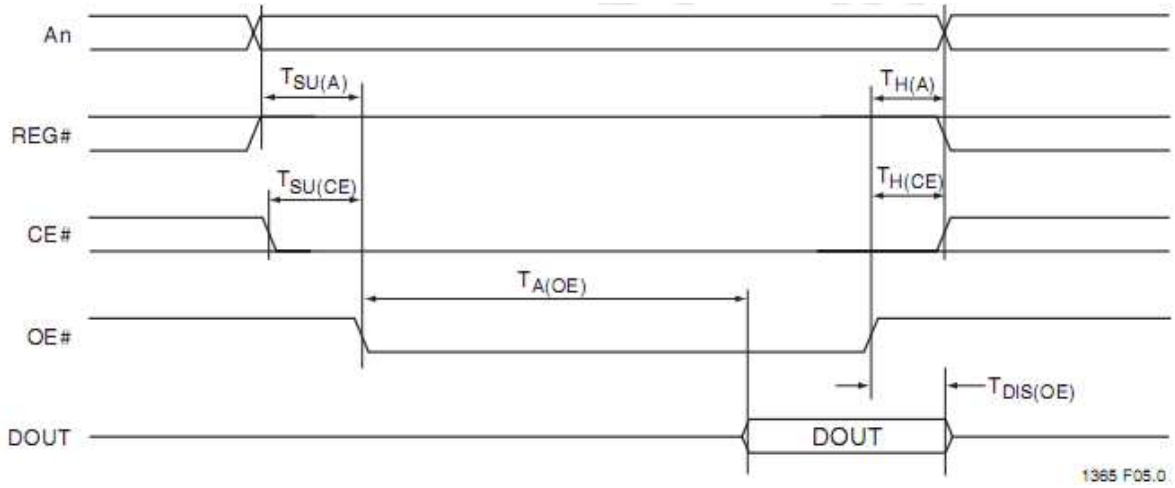


Figure 7-4: Common Memory Read Timing Diagram

7.2.4 Common Memory Write Timing Specification

Table 7-8 Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min[1]	Min[1]	Units
Data Setup before WE	$T_{SU(DWE\#H)}$	tDVWH	40		ns
Data Hold following WE	$T_{H(D)}$	tWMDX	15		ns
WE Pulse Width	$T_{W(WE)}$	tWLWH	60		ns
Address Setup Time	$T_{SU(A)}$	tAVWL	10		ns
CE Setup before WE	$T_{SU(CE)}$	tELWL	0		ns
Write Recovery Time	$T_{REC(WE)}$	tWMAX	15		ns
Address Hold Time	$T_{H(A)}$	tGHAX	15		ns
CE Hold following WE	$T_{H(CE)}$	tGHEH	15		ns

1. All AC specifications are guaranteed by design.

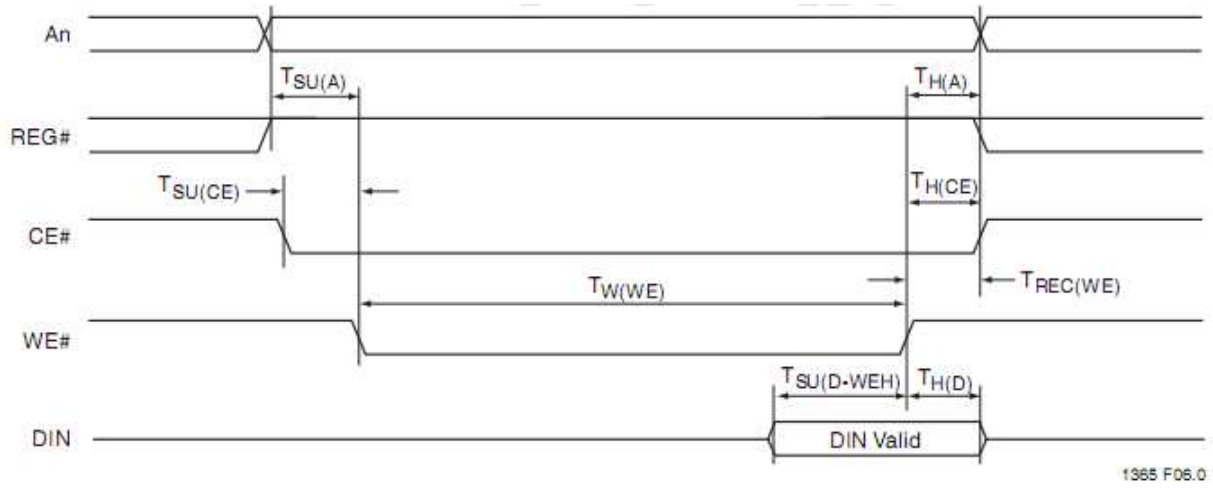


Figure 7-5: Common Memory Write Timing Diagram

7.2.5 I/O Input (Read) Timing Specification

Table 7-9 I/O Read Timing

Item	Symbol	IEEE Symbol	Min[1]	Min[1]	Units
Data Delay after IORD	$T_{D(IORD)}$	tIGLQV		100	ns
Data Hold following IORD	$T_{H(IORD)}$	tIGHQX	0		ns
IORD Width Time	$T_{W(IORD)}$	tIGLIGH	165		ns
Address Setup before IORD	$T_{SUA(IORD)}$	tAVIGL	70		ns
Address Hold following IORD	$T_{HA(IORD)}$	tIGHAX	20		ns
CE Setup before IORD	$T_{SUCE(IORD)}$	tELIGL	5		ns
CE Hold following IORD	$T_{HCE(IORD)}$	tIGHEH	20		ns
REG Setup before IORD	$T_{SUREG(IORD)}$	tRGLIGL	5		ns
REG Hold following IORD	$T_{HREG(IORD)}$	tIGHRGH	0		ns
INPACK Delay Falling from IORD	$T_{DFINPACK(IORD)}$	tIGLIAL	0	45	ns
INPACK Delay Rising from IORD	$T_{DRINPACK(IORD)}$	tIGHIAH		45	ns
IOIS16 Delay Falling from Address	$T_{DFIOIS16(ARD)}$	tAVISL		35	ns
IOIS16 Delay Rising from Address	$T_{DRIOIS16(ADR)}$	tAVISH		35	ns

1. All AC specifications are guaranteed by design.
Note: The maximum load on –INPACK and IOIS16# is 1 LSTTL with 50pF total load.

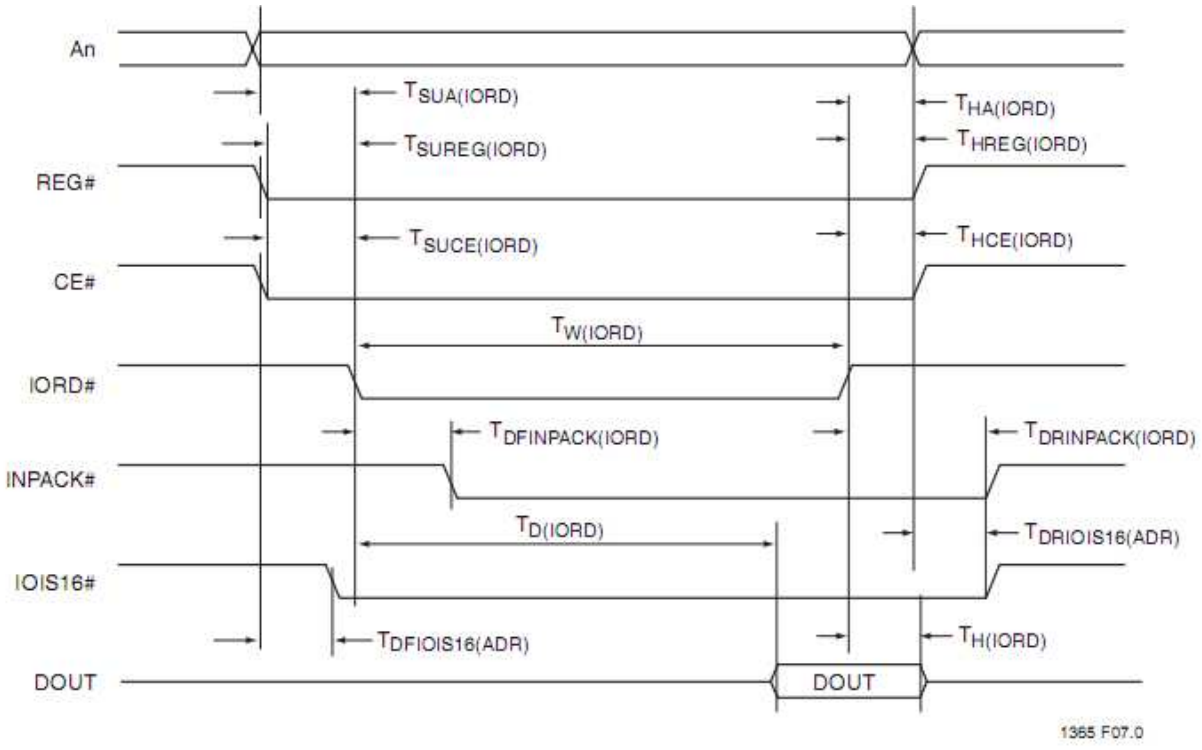


Figure 7-6: I/O Read Timing Diagram

7.2.6 I/O Output (Write) Timing Specification

Table 7-10 I/O Write Timing

Item	Symbol	IEEE Symbol	Min[1]	Min[1]	Units
Data Setup before IOWR	$T_{SU(IOWR)}$	tDVIWH	60		ns
Data Hold following IOWR	$T_{H(IOWR)}$	tIWHDX	30		ns
IOWR Width Time	$T_{W(IOWR)}$	tIWLIWH	165		ns
Address Setup before IOWR	$T_{SUA(IOWR)}$	tAVIWL	70		ns
Address Hold following IOWR	$T_{HA(IOWR)}$	tIWHAX	20		ns
CE Setup before IOWR	$T_{SUCE(IOWR)}$	tELIWL	5		ns
CE Hold following IOWR	$T_{HCE(IOWR)}$	tIWHEH	20		ns
REG Setup before IOWR	$T_{SUREG(IOWR)}$	tRGLIWL	5		ns
REG Hold following IOWR	$T_{HREG(IOWR)}$	tIWHRGH	0		ns
IOIS16 Delay Falling from Address	$T_{DFIOIS16(ARD)}$	tAVISL		35	ns
IOIS16 Delay Rising from Address	$T_{DRIOIS16(ADR)}$	tAVISH		35	ns

1. All AC specifications are guaranteed by design.
Note: The maximum load on –INPACK and IOIS16# is 1 LSTTL with 50pF total load.

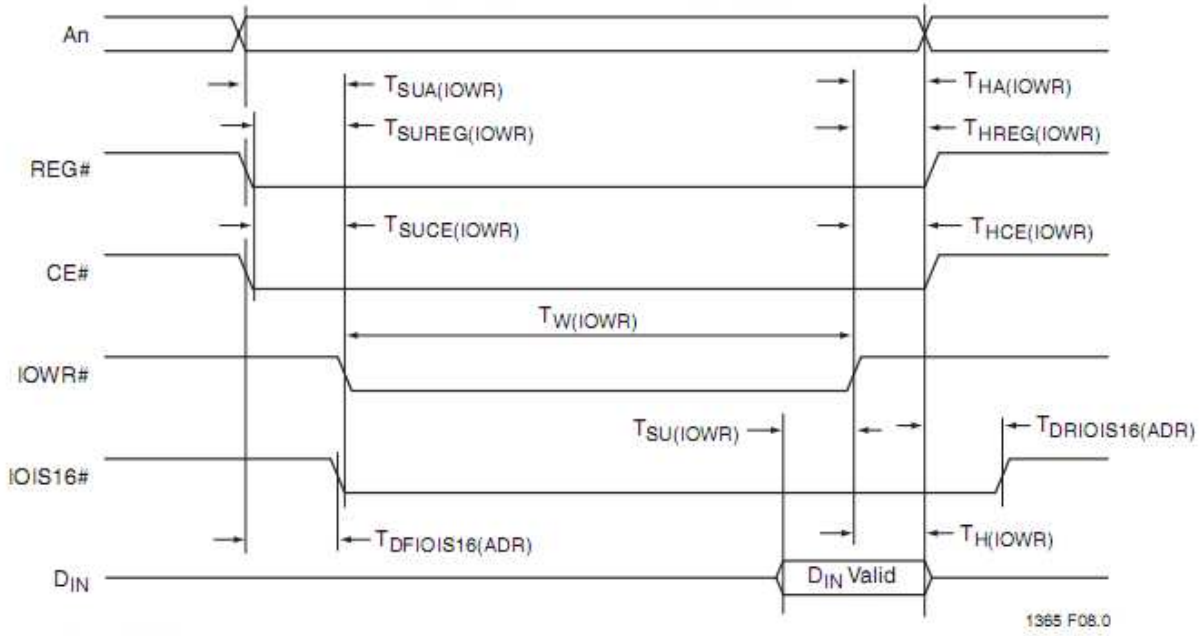


Figure 7-7: I/O Write Timing Diagram

7.2.7 Ultra DMA Mode Data Transfer Input/Output (Read/Write) Timing

Table 7-11 Ultra DMA Data Burst Timing Specifications[1]

Name	Descriptions	Mode 4		Unit	Measurement Location[2]
		Min	Max		
$T_{2CYCTYP}$	Typical sustained average two cycle time	60		ns	Sender
T_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	25		ns	Note[3]
T_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	57		ns	Sender
T_{DS}	Data setup time at recipient (from data valid until STROBE edge)[4,5]	5.0		ns	Recipient
T_{DH}	Data hold time at Recipient (from STROBE edge until data becomes invalid)[1,2]	5.0		ns	Recipient
T_{DVS}	Data valid setup time for Sender (from data valid until STROBE edge)[6]	6.0		ns	Sender
T_{DVH}	Data valid hold time at Sender (from STROBE edge until data becomes invalid)[3]	6.0		ns	Sender
T_{CS}	CRC word setup time at device[1]	5.0		ns	Device
T_{CH}	CRC word hold time at device[1]	5.0		ns	Device
T_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK negation)[3]	6.7		ns	Host
T_{CVH}	CRC word valid hold time at Sender (from DMACK negation until CRC becomes invalid)[3]	6.2		ns	Host
T_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	0		ns	Device
T_{DZFS}	Time from data output released-to-driving until the first transition of critical timing	6.7		ns	Sender
T_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)		120	ns	Device
T_{LI}	Limited interlock time[7]	0	100	ns	Note[8]
T_{MLI}	Interlock time with minimum[4]	20		ns	Host
T_{UI}	Unlimited interlock time[4]	0		ns	Host
T_{AZ}	Maximum time allowed for output drivers to release (from asserted to negated)		10	ns	Note[9]
T_{ZAH}	Minimum delay time required for output	20		ns	Host
T_{ZAD}	Drivers to assert or negate (from released)	0		ns	Device
T_{ENV}	Envelope time (from DMACK# to STOP and HDMARDY# during data in burst initiation and from DMACK to STOP during data our burst initiation)	20	55	ns	Host
T_{RFS}	Ready-to-final STROBE time (no STROBE edge are sent this long after negation of DMARDY)		60	ns	Sender
T_{RP}	Ready-to-pause time (Recipient waits to pause until after negating DMARDY)	100		ns	Recipient
T_{IORDYZ}	Maximum time before releasing IORDY		20	ns	Device
T_{ZIORDY}	Minimum time before driving IORDY[10]	0		ns	Device
T_{ACK}		20		ns	Host
T_{SS}		50		ns	Sender

4. All timing measurement switching points (low-to-high and high-to-low) are taken at 1.5V.
5. All signal transitions for a timing parameter are measured at the connector specified in the measurement location column. For example, in the case of TRFS, both STROBE and DMARDY Transitions are measured at the Sender connector.
6. The parameter TCYC is measured at the recipient's connector farthest from the Sender.
7. 80-Conductor cabling is required in order to meet sup (TDS, TCS) and hold (TDH, TCH) times in modes greater than two.
8. The parameters TDS and TDH for Mode 5 are defined for a Recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for TDS and TDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.
9. Timing for TDVS, TDVH, TCVS, and TCVH are met for lumped capacitive loads of 15 and 50 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
10. The parameters TUI, TMLI, and TLI indicate Sender-to-Recipient or Recipient-to-Sender interlocks. For example, one agent (either Sender or Recipient) is waiting for the other agent to respond with a signal before proceeding; TUI is an unlimited interlock that has no maximum time value, TMLI is a limited time-out that has a defined minimum, and TLI is a limited time-out that has a defined maximum.
11. The parameter TLI is measured at the connector of the Sender or Recipient that is responding to an incoming transition from the Recipient or Sender respectively. Both the incoming signal and the outgoing response are measured at the same connector.
12. The parameter TAZ is measured at the connector of the Sender or Recipient that is driving the bus but must release the bus that allow for a bus turnaround.
13. For all modes the parameter TZIORDY may be greater than TENV because the host has a pull-on IORDY giving it a known state when released.

Table 7-12 Ultra DMA Sender and Recipient IC Timing Specifications[1]

Name	Descriptions	Mode 4		Unit
		Min	Max	
T_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge)[2]	4.8		ns
T_{DHIC}	Recipient IC data hold time (from STROBE edge until data becomes invalid)[1]	4.8		ns
T_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge)[3]	9.5		ns
T_{DVHIC}		9.0		ns

1. All timing measurement switching point (low-to-high and high-to-low)
2. The correct data value is captured by the Recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at TDSIC and TDHIC timing (as measured through 1.5 V).
3. The parameters TDVSIC and TDVHIC are met for lumped capacitive loads of 15 and 40 pf at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

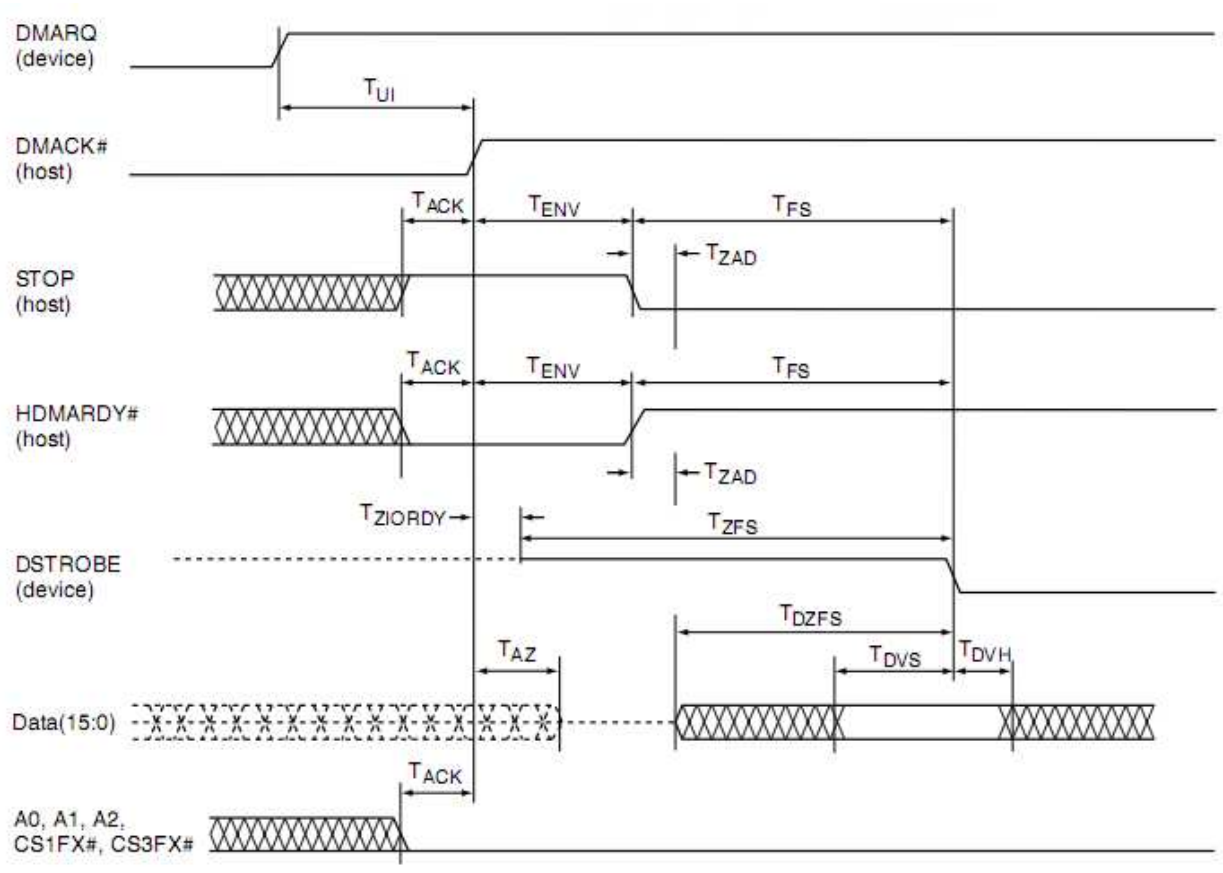


Figure 7-8: Initiating an Ultra DMA Data-In Burst

Notes:
1. The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDRARDY-: DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

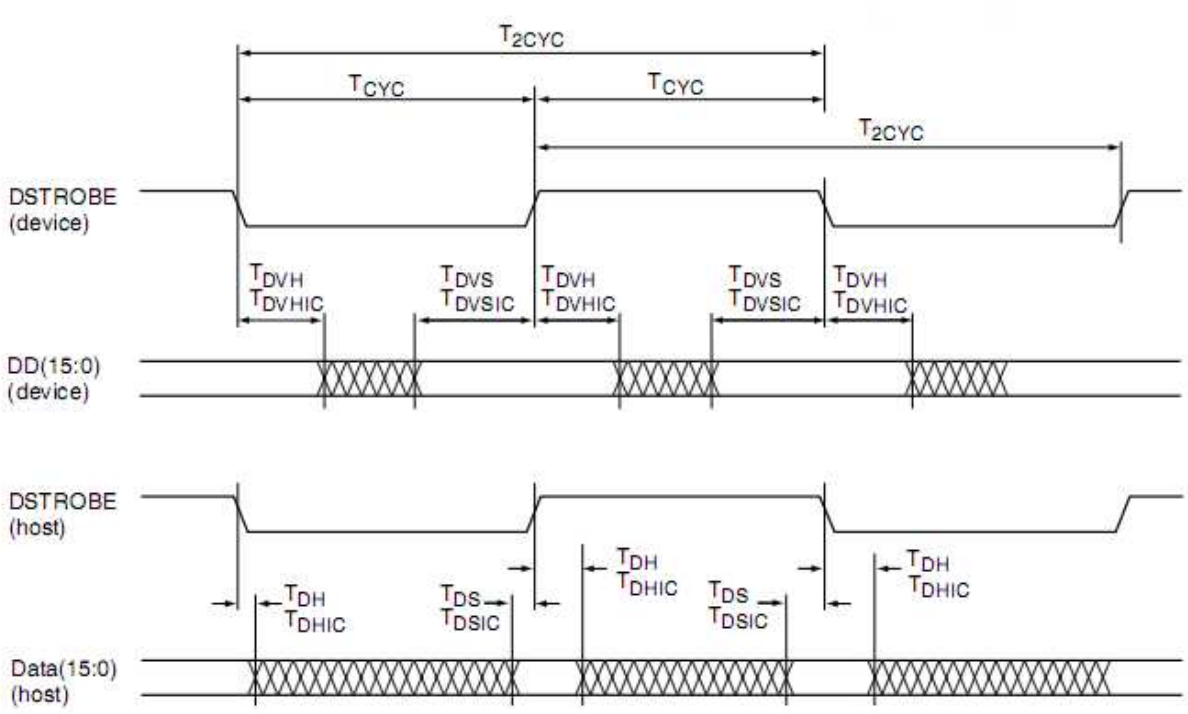


Figure 7-9: Sustained Ultra DMA Data-In Burst

Notes:

1. DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the device.

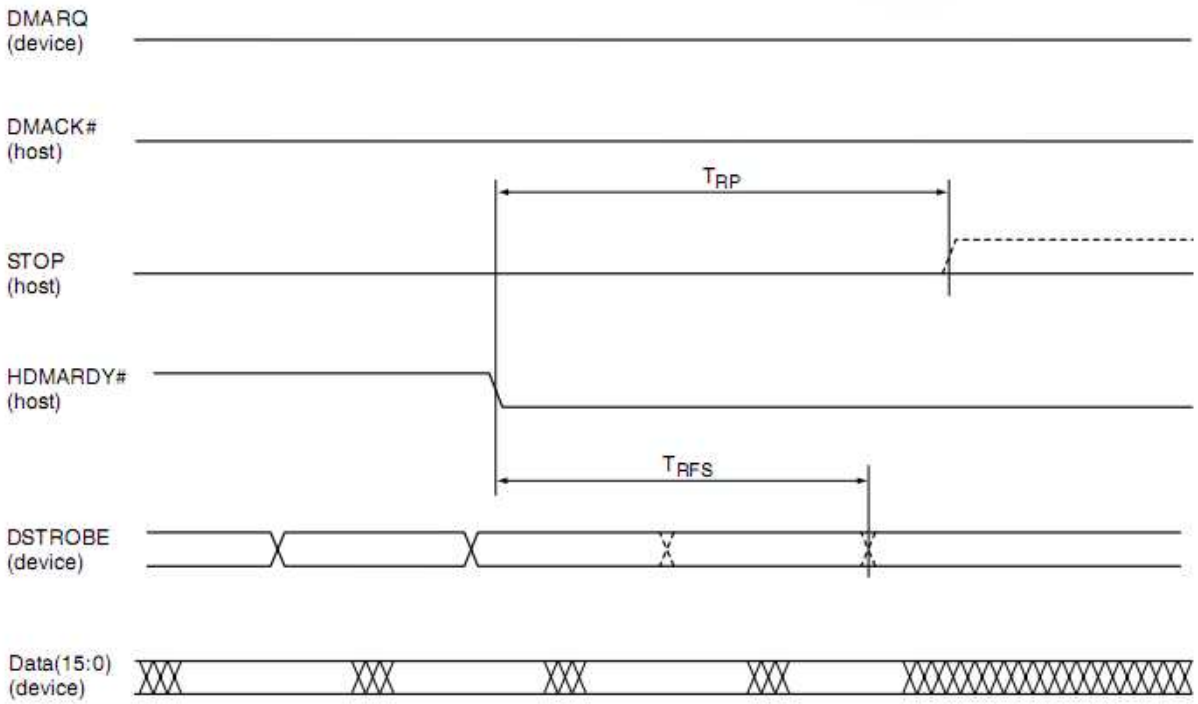


Figure 7-10: Sustained Ultra DMA Data-In Burst

Notes:
1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than TRP after HDMARDY# is negated.
2. After negating HDMARDY#, the host may receive zero, one, two, or three more data words from the device.

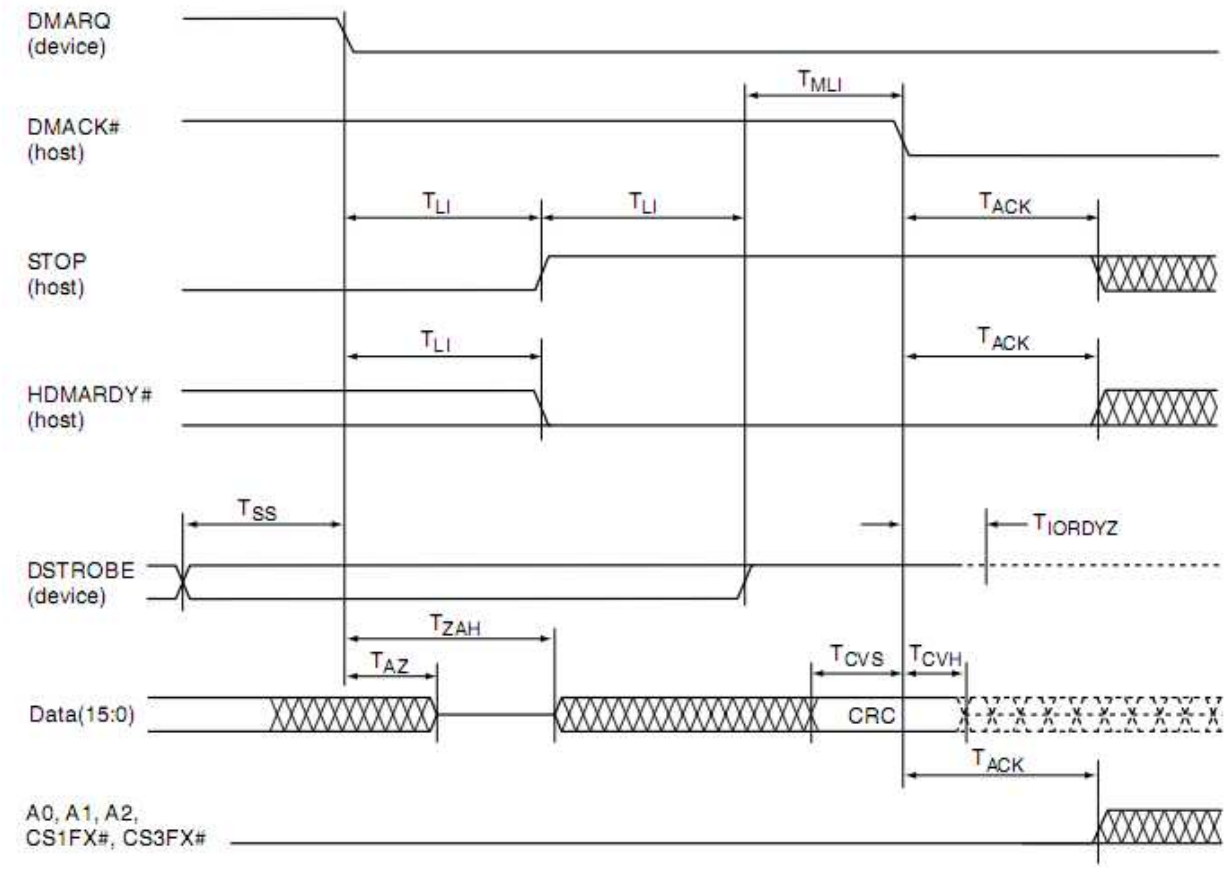


Figure 7-11: Device Terminating and Ultra DMA Data-In Burst

Notes:
1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

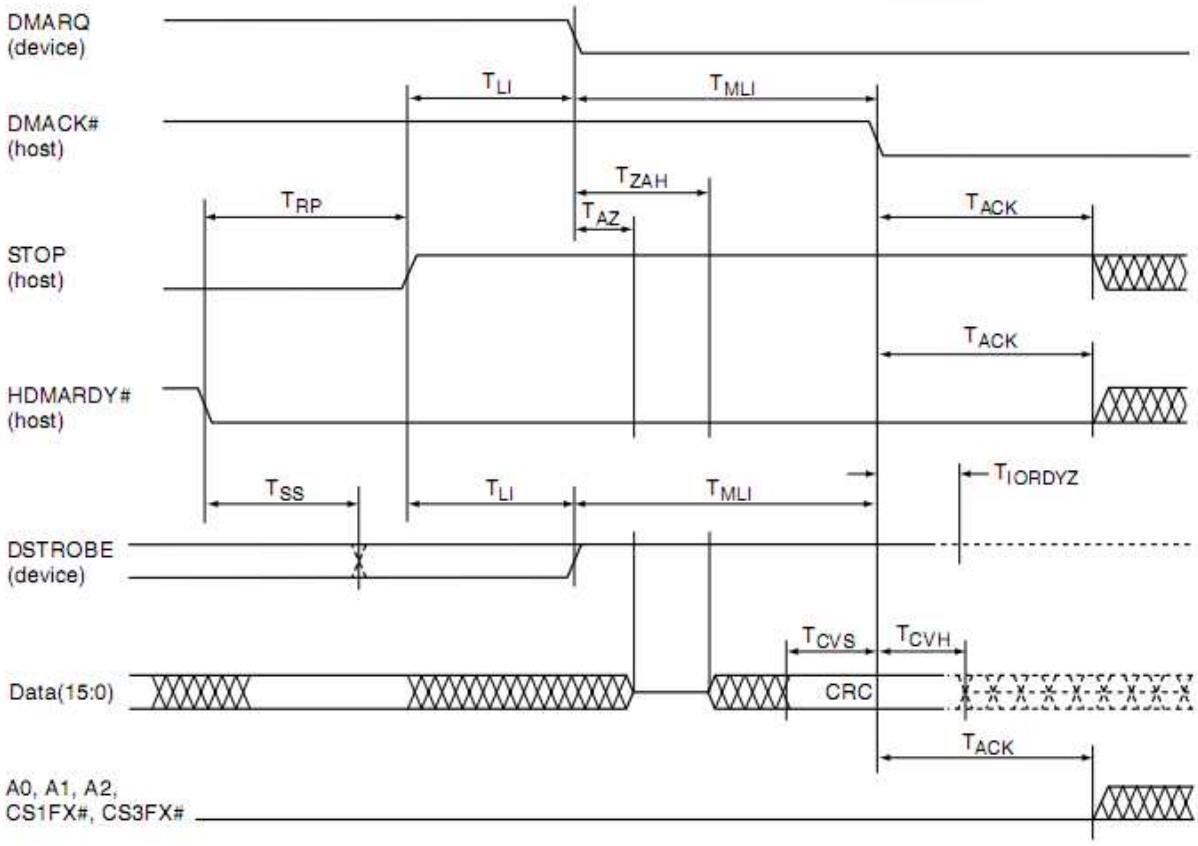


Figure 7-12: Host Terminating and Ultra DMA Data-In Burst

Notes:
1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

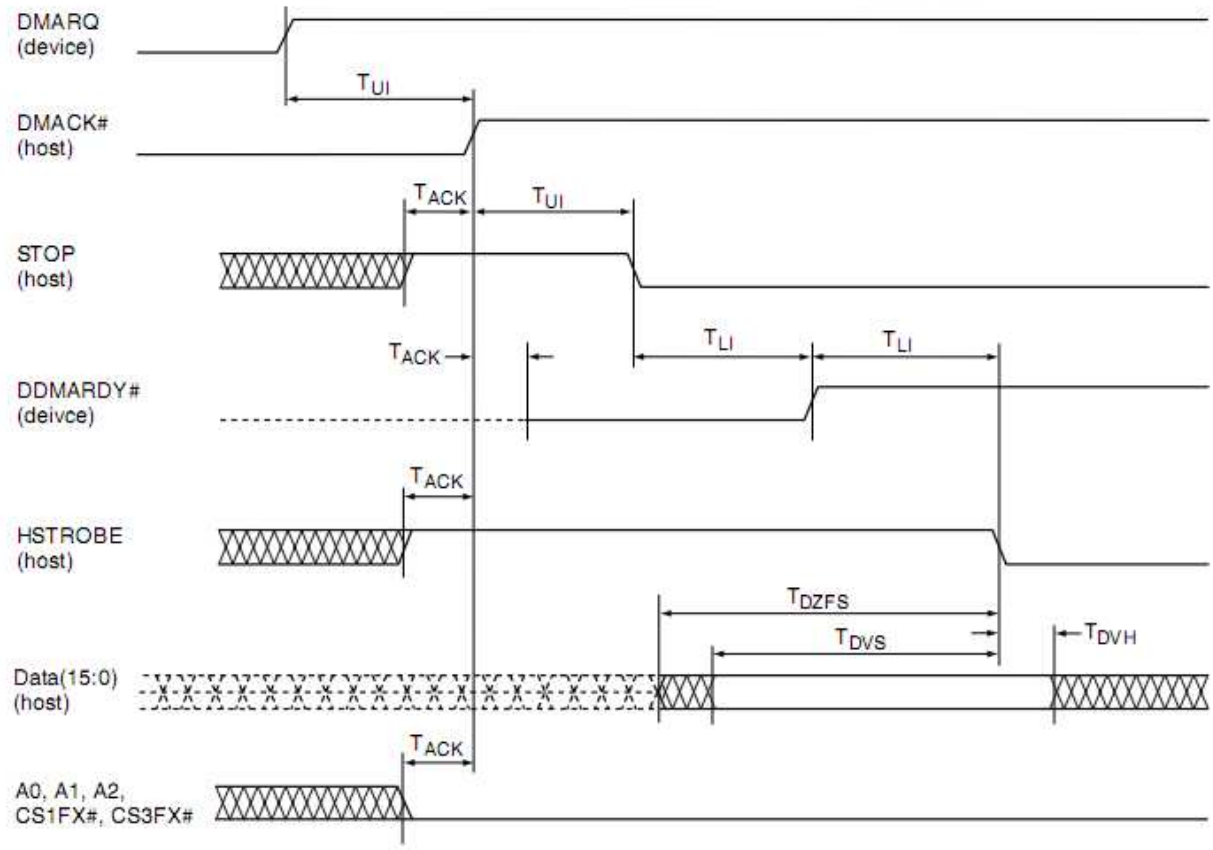


Figure 7-13: Initiating an Ultra DMA Data-Out Burst

Notes:
1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

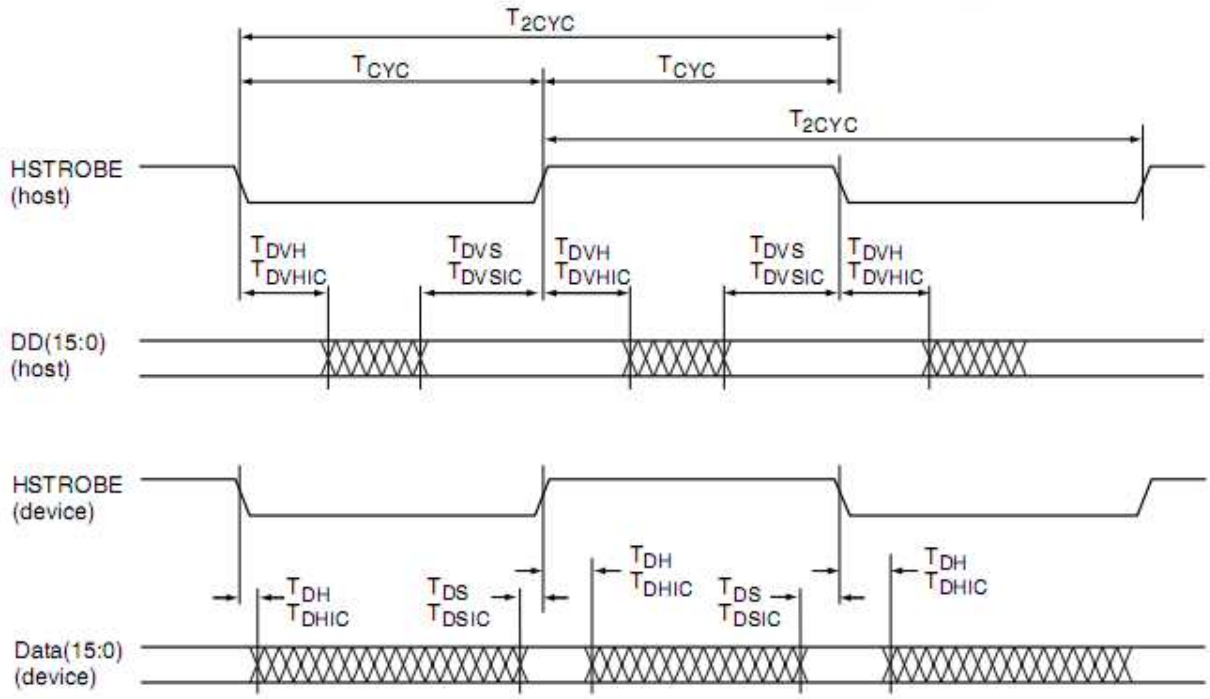


Figure 7-14: Sustained Ultra DMA Data-Out Burst

Notes:

1. DD(15:0) and HSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the host.

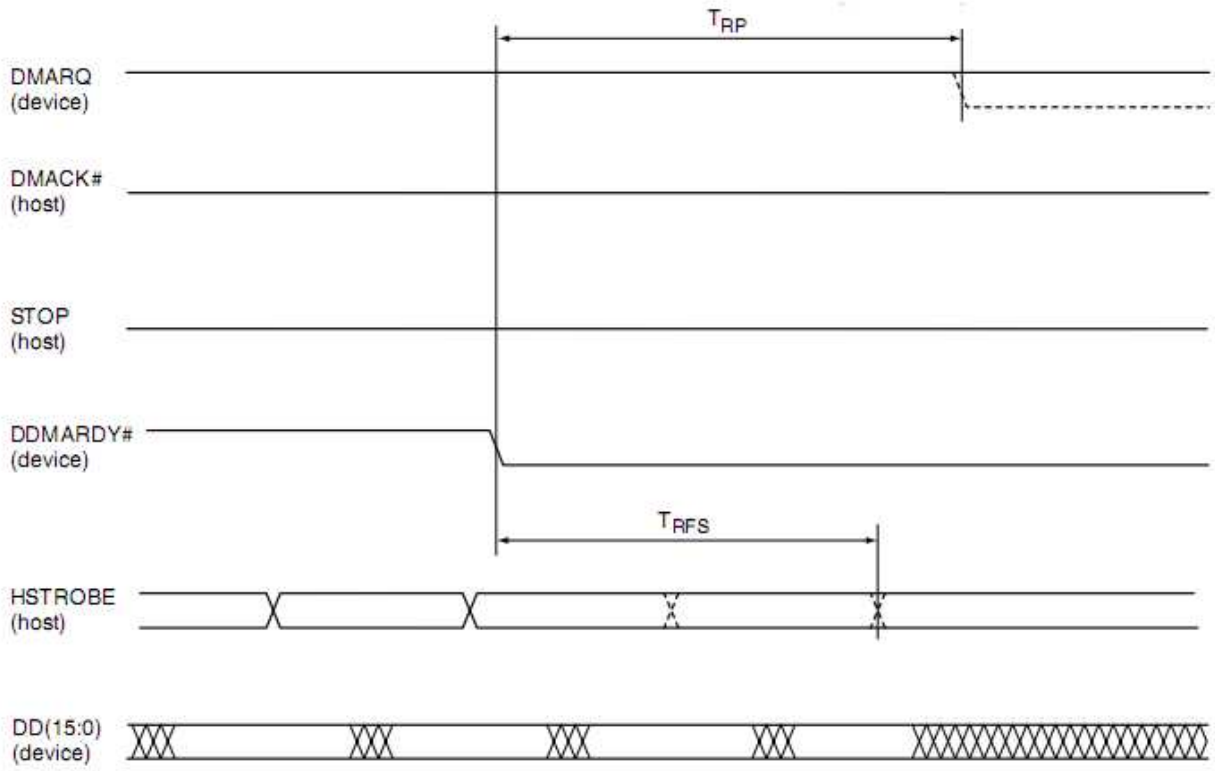


Figure 7-15: Device Pausing and Ultra DMA Data-Out Burst

Notes:
1. The host may negate DMARQ to request termination of the Ultra DMA burst no sooner than TRP after DDMARDY# is negated.
2. After negating DDMARDY#, the host may receive zero, one, two, or three more data words from the host.

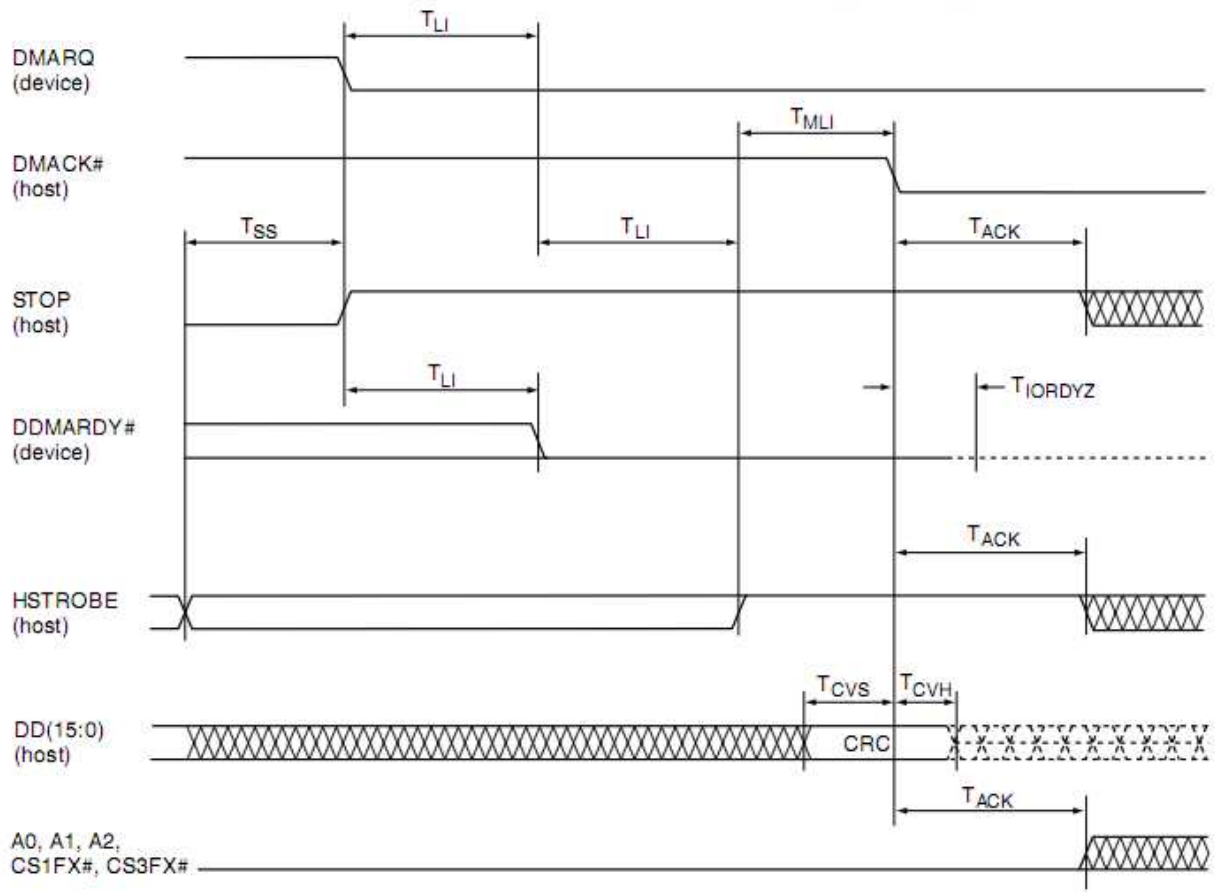


Figure 7-16: Host Terminating and Ultra DMA Data-Out Burst

Notes:

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

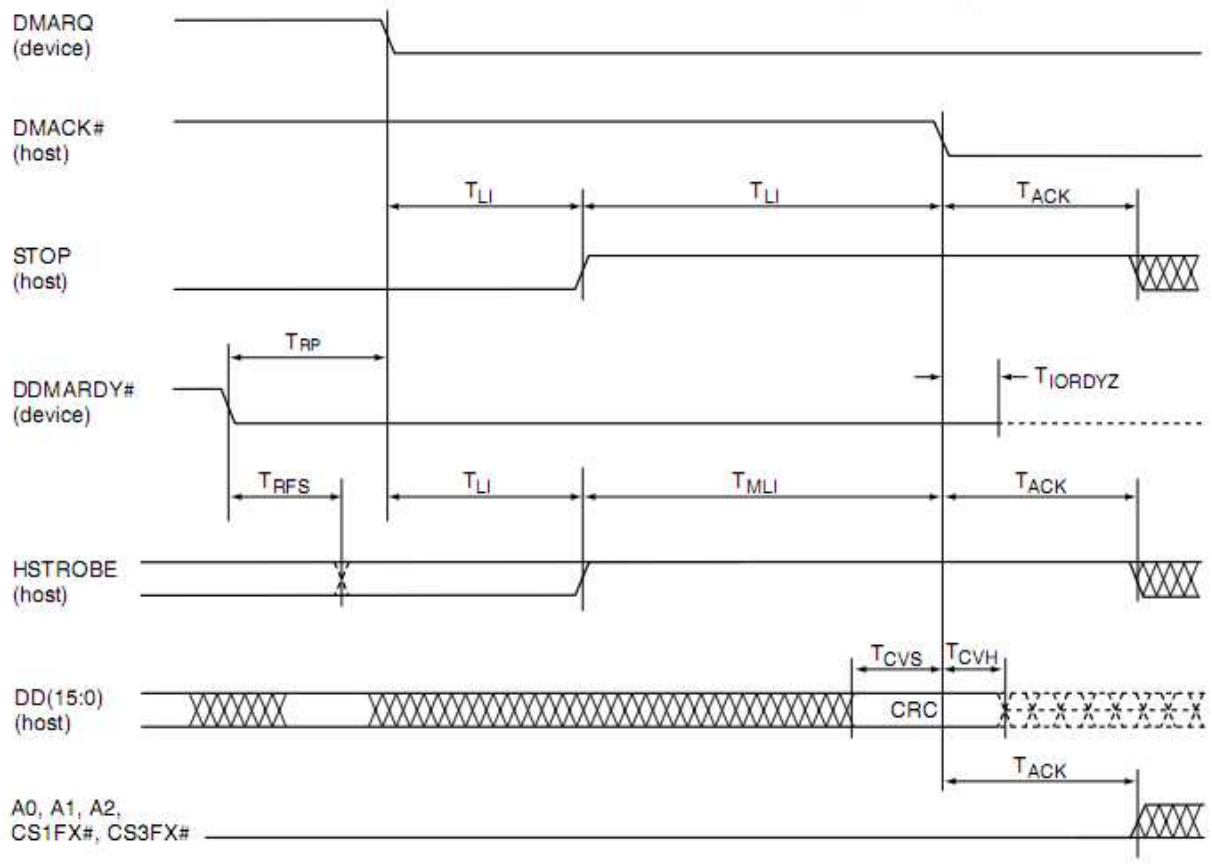


Figure 7-17: Device Terminating and Ultra DMA Data-Out Burst

Notes:
1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

7.2.8 Media Side Interface I/O Timing Specifications

Table 7-13: Timing Parameter

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	20	-	ns
T_{CLH}	FCLE Hold Time	40	-	ns
T_{CS}	FCE# Setup Time	40	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	40	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	-	40	ns
T_{WP}	FWE# Pulse Width	20	-	ns
T_{WH}	FWE# High Hold Time	20	-	ns
T_{WC}	Write Cycle Time	40	-	ns
T_{ALS}	FALE Setup Time	20	-	ns
T_{ALH}	FALE Hold Time	40	-	ns
T_{DS}	FAD[15:0] Setup Time	20	-	ns
T_{DH}	FAD[15:0] Hold Time	20	-	ns
T_{RP}	FRE# Pulse Width	20	-	ns
T_{RR}	Ready to FRE# Low	40	-	ns
T_{RES}	FRE# Data Setup Access Time	20	-	ns
T_{RC}	Read Cycle Time	40	-	ns
T_{REH}	FRE# High Hold Time	20	-	ns
T_{RHZ}	FRE# High to Data Hi-Z	5	-	ns

Note: All AC specifications are guaranteed by design.

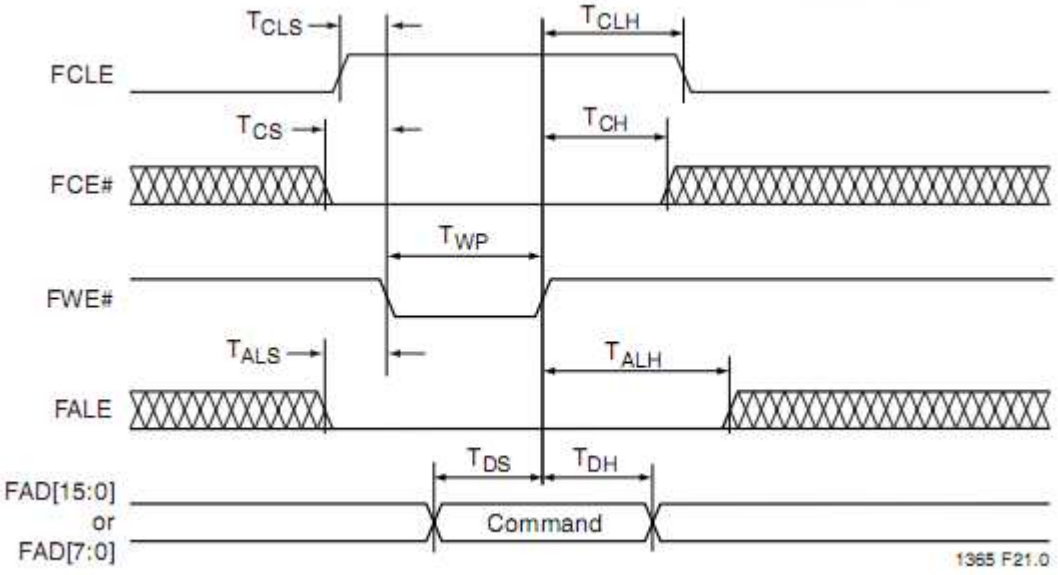


Figure 7-18: Media Command Latch Cycle

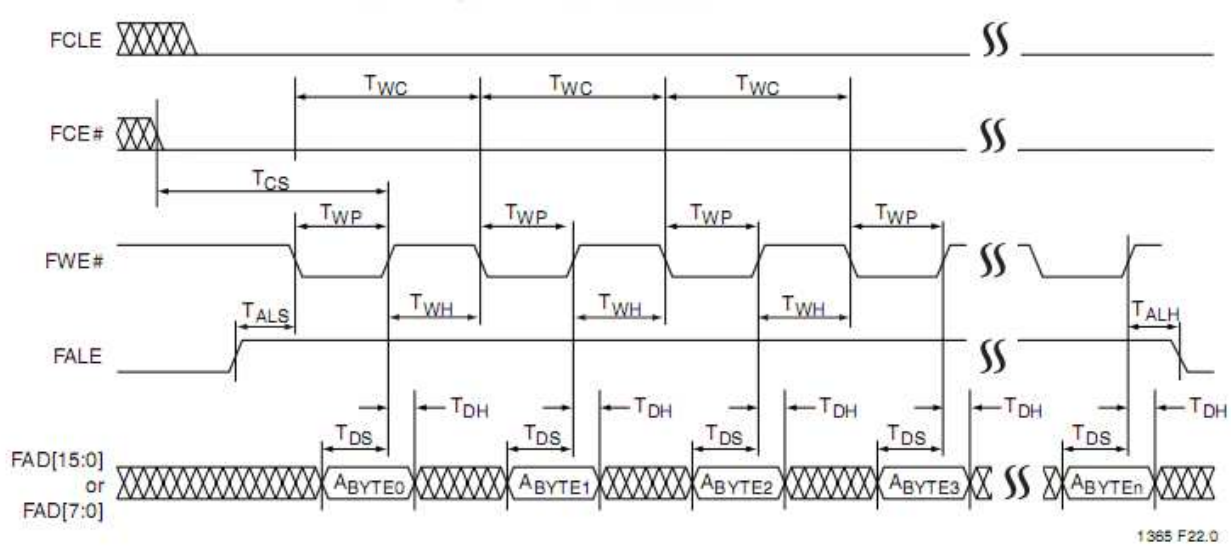


Figure 7-19: Media Access Latch Cycle

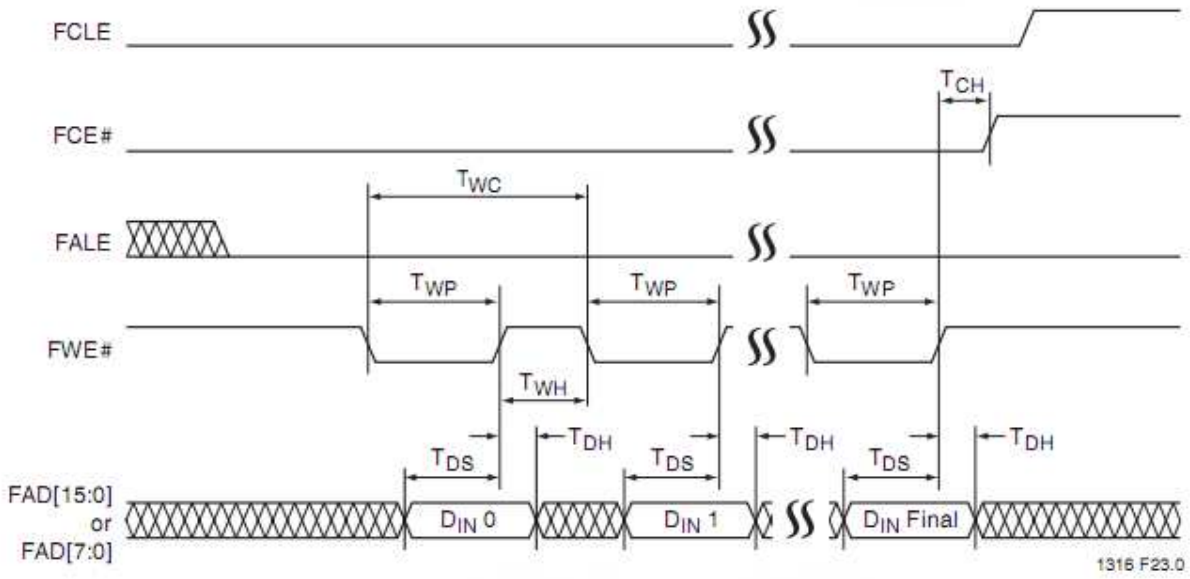


Figure 7-20: Media Data Loading Latch Cycle

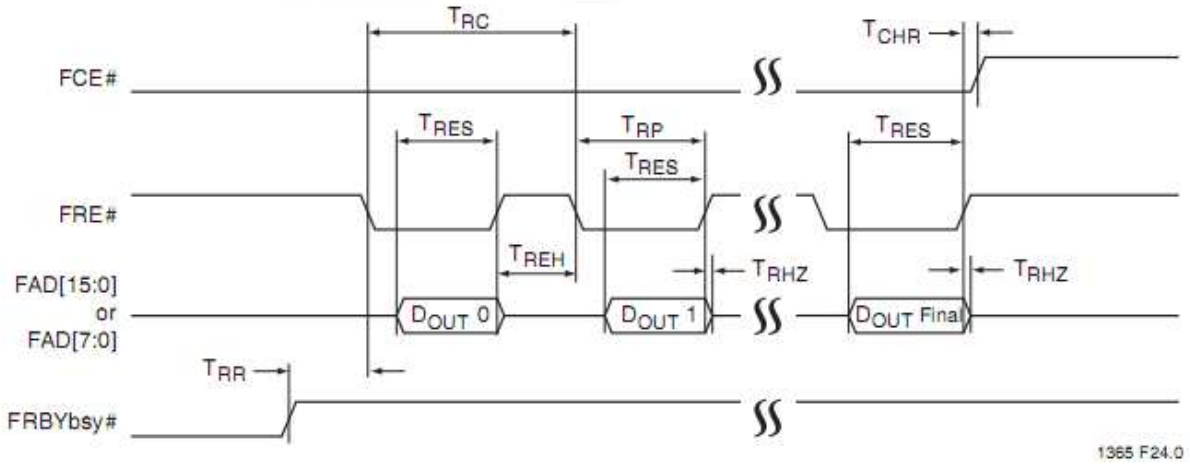


Figure 7-21: Media Data Read Cycle

8. Physical Characteristics

8.1 Dimension

TABLE 8-1: Type I CFC physical specification

Length:	36.40 +/- 0.15mm (1.433+/- 0.06 in.)
Width:	42.80 +/- 0.10mm (1.685+/- 0.04 in.)
Thickness (Including Label Area):	3.3mm+/-0.10mm (0.130+/-0.04in.)

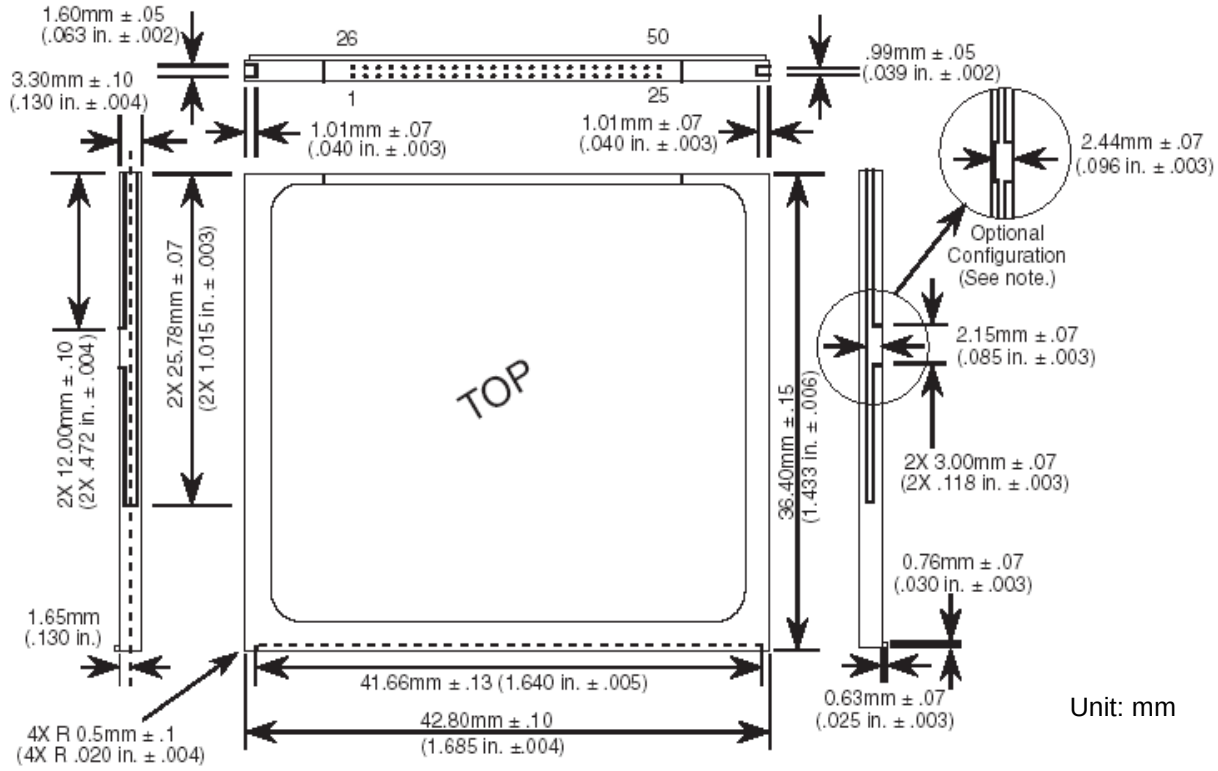
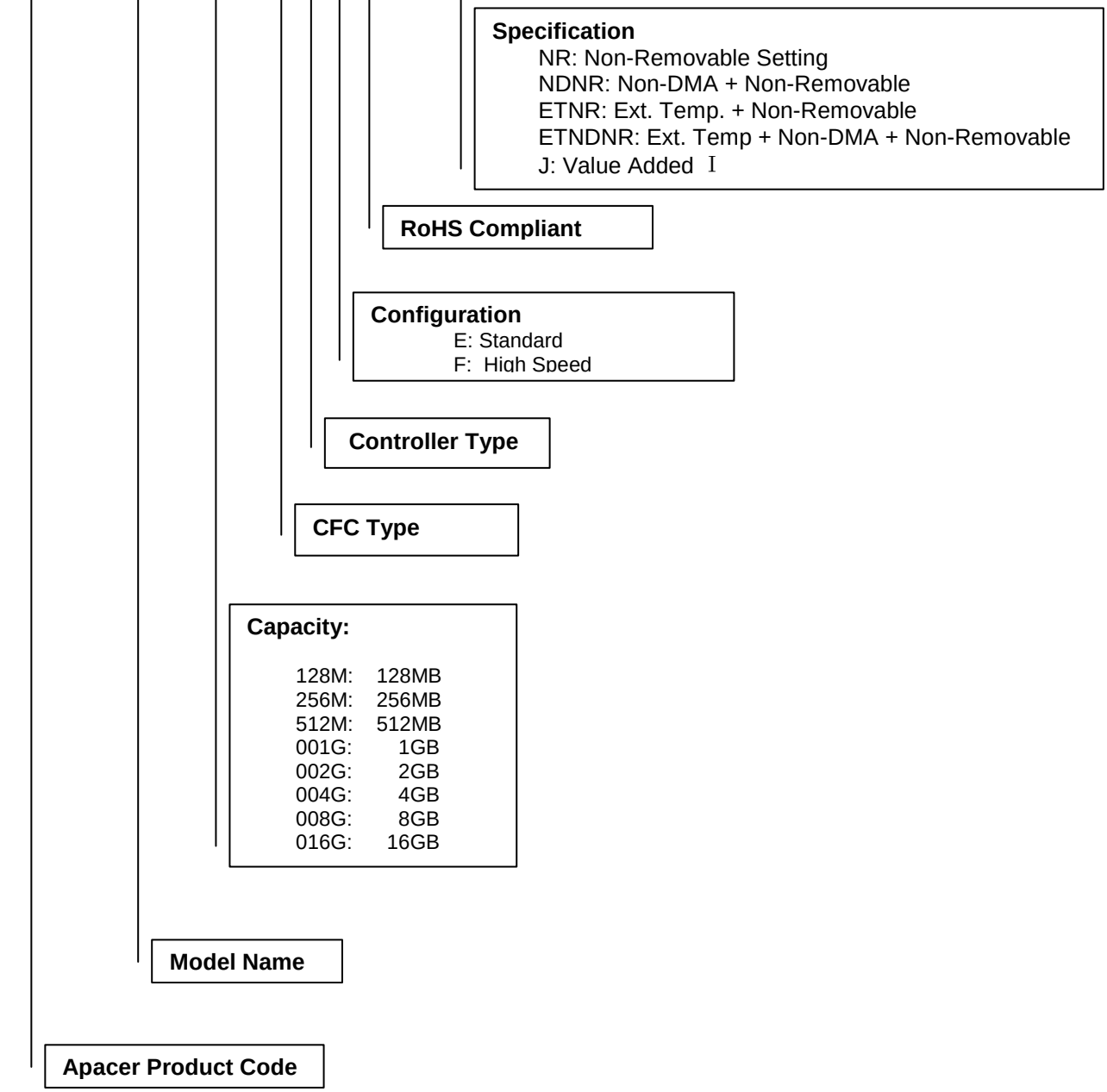


FIGURE 8-1: Physical dimension

9. Product Ordering Information

9.1 Product Code Designations

A P – C F x x x x E 3 X R – XXXXJ



9.2 Valid Combinations

Standard Temperature

Non-Removable

Standard Speed **High Speed**

Capacity	Model Number	Capacity	Model Number
128MB	AP-CF128ME3ER-NRJ	256MB	AP-CF256ME3FR-NRJ
256MB	AP-CF256ME3ER-NRJ	512MB	AP-CF512ME3FR-NRJ
512MB	AP-CF512ME3ER-NRJ	1GB	AP-CF001GE3FR-NRJ
1GB	AP-CF001GE3ER-NRJ	2GB	AP-CF002GE3FR-NRJ
2GB	AP-CF002GE3ER-NRJ	4GB	AP-CF004GE3FR-NRJ
16GB	AP-CF016GE3ER-NRJ	8GB	AP-CF008GE3FR-NRJ

Non-DMA & Non-Removable

Standard Speed **High Speed**

Capacity	Model Number	Capacity	Model Number
128MB	AP-CF128ME3ER-NDNRJ	256MB	AP-CF256ME3FR-NDNRJ
256MB	AP-CF256ME3ER-NDNRJ	512MB	AP-CF512ME3FR-NDNRJ
512MB	AP-CF512ME3ER-NDNRJ	1GB	AP-CF001GE3FR-NDNRJ
1GB	AP-CF001GE3ER-NDNRJ	2GB	AP-CF002GE3FR-NDNRJ
2GB	AP-CF002GE3ER-NDNRJ	4GB	AP-CF004GE3FR-NDNRJ
16GB	AP-CF016GE3ER-NDNRJ	8GB	AP-CF008GE3FR-NDNRJ

Extended Temperature

Non-Removable

Standard Speed **High Speed**

Capacity	Model Number	Capacity	Model Number
128MB	AP-CF128ME3ER-ETNRJ	256MB	AP-CF256ME3FR-ETNRJ
256MB	AP-CF256ME3ER-ETNRJ	512MB	AP-CF512ME3FR-ETNRJ
512MB	AP-CF512ME3ER-ETNRJ	1GB	AP-CF001GE3FR-ETNRJ
1GB	AP-CF001GE3ER-ETNRJ	2GB	AP-CF002GE3FR-ETNRJ
2GB	AP-CF002GE3ER-ETNRJ	4GB	AP-CF004GE3FR-ETNRJ
16GB	AP-CF016GE3ER-ETNRJ	8GB	AP-CF008GE3FR-ETNRJ

Non-DMA & Non-Removable

Standard Speed **High Speed**

Capacity	Model Number	Capacity	Model Number
128MB	AP-CF128ME3ER-ETNDNRJ	256MB	AP-CF256ME3FR-ETNDNRJ
256MB	AP-CF256ME3ER-ETNDNRJ	512MB	AP-CF512ME3FR-ETNDNRJ
512MB	AP-CF512ME3ER-ETNDNRJ	1GB	AP-CF001GE3FR-ETNDNRJ
1GB	AP-CF001GE3ER-ETNDNRJ	2GB	AP-CF002GE3FR-ETNDNRJ
2GB	AP-CF002GE3ER-ETNDNRJ	4GB	AP-CF004GE3FR-ETNDNRJ
16GB	AP-CF016GE3ER-ETNDNRJ	8GB	AP-CF008GE3FR-ETNDNRJ

Revision History

Revision	Date	Description	Remark
1.0	12/30/2008	Official release	
1.1	01/08/2009	Context revised	
1.2	02/11/2009	Modified document layout	
1.3	03/10/2009	Updated valid combination	
1.4	03/26/2009	Updated valid combination wording & performance table	
1.5	04/12/2009	Updated electrical specifications & capacity	
1.6	06/16/2009	Updated pin assignment	

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