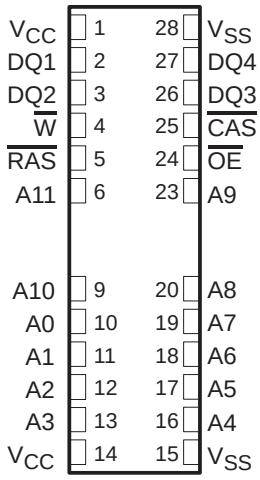
- **Organization . . . 4194304 × 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

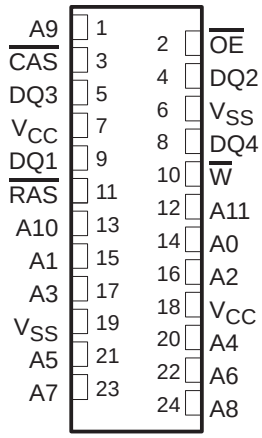
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'416400-70	70 ns	18 ns	35 ns	130 ns
'416400-80	80 ns	20 ns	40 ns	150 ns
'416400-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  4096 Cycles Refresh in 32 ms
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs, and Clocks are TTL-Compatible**
- **Operating Free-Air Temperature Range**
  – 55°C to 125°C

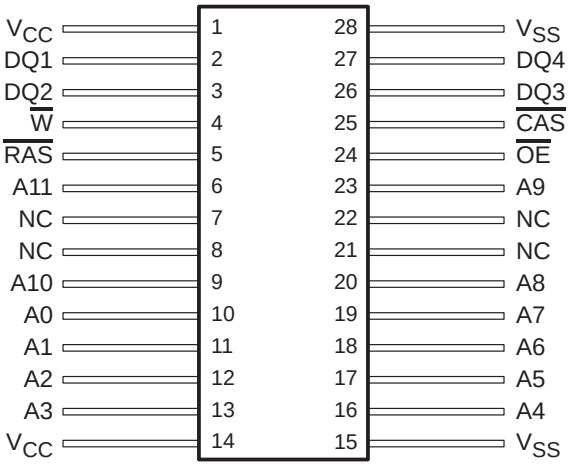
FNC PACKAGE
(TOP VIEW)



SV PACKAGE
(TOP VIEW)



HKB PACKAGE
(TOP VIEW)



description

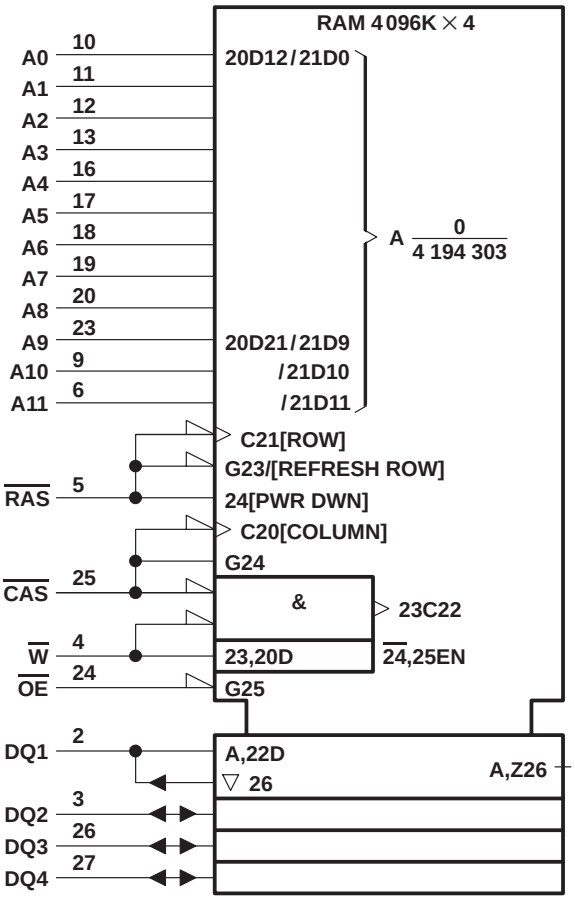
The SMJ416400 series is a set of high-speed 16777216-bit dynamic random-access memories (DRAMs), organized as 4194304 words of four bits each. The series employs technology for high performance, reliability, and low power.

These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. All inputs, outputs, and clocks are compatible with series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ416400 is offered in 450-mil 24/28-pin surface-mount small-outline leadless chip carrier (FNC suffix), 28-lead flatpack (HKB suffix), and 24-lead ZIP (SV suffix) packages. The packages are characterized for operation from –55°C to 125°C.

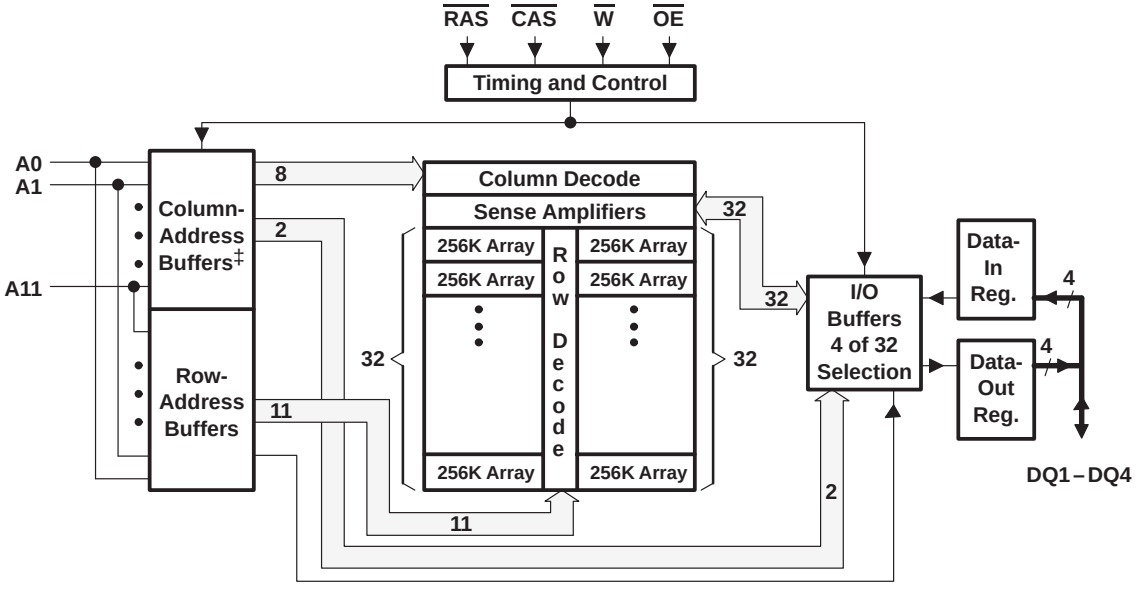
PIN NOMENCLATURE	
$\overline{A0}$–$\overline{A11}$	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FNC and HKB packages.

functional block diagram



‡ Column address 10 and column address 11 are not used.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address and strobing random column addresses onto the chip. The time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The column-address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output-enable. This feature allows the SMJ416400 to operate at a higher data bandwidth than conventional page-mode parts because retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ goes low. The performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{CAS}$ low) if t_{AA} maximum (access time from column address) and t_{OEA} have been satisfied. When the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0 – A11)

Twenty-two address bits are required to decode one of 4194304 storage-cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched onto the chip by the row-address strobe, $\overline{RAS}$. Ten column-address bits are set on A0 through A9 and latched onto the chip by the column-address strobe, $\overline{CAS}$. Row address A11 is required during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip-enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting a write operation that is independent of the state of $\overline{OE}$. This permits an early-write operation to be completed with $\overline{OE}$ grounded.

data in/data out (DQ1 – DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ is already low; data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two series 54 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to the high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. Both $\overline{RAS}$ and $\overline{CAS}$ must be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, the output buffers remain in this state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and by cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden-refresh cycle. An internal-refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is used by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . – 55°C to 125°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'416400-70		'416400-80		'416400-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		80		70		60	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.05 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)†	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		80		70		60	mA
I_{CC4}	Average page current (see Note 4)†	$\overline{RAS}$ low, $\overline{CAS}$ cycling		65		60		55	mA
I_{CC7}	Standby current output enable†	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

† Minimum cycle, V_{CC} = 5.5 V

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0 – A11‡		9	pF
$C_{i(RC)}$	Input capacitance, $\overline{RAS}$ and $\overline{CAS}$‡		8	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$‡		8	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$‡		8	pF
C_o	Output capacitance		14	pF

‡ Input capacitance for ZIP (SV suffix) package is 12 pF.

NOTE 5: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 6)

PARAMETER		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		18		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20		25	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	18	0	20	0	25	ns

NOTES: 6. Valid data is presented at the outputs after all access times are satisfied but can go from the high-impedance state to an invalid-data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.
7. t_{OFF} and t_{OEZ} are specified when the outputs are no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	130		150		180		ns
t_{RWC}	Cycle time, read-write (see Note 8)	181		205		245		ns
t_{PC}	Cycle time, page mode read or write (see Notes 8 and 9)	45		50		55		ns
t_{PRWC}	Cycle time, page mode read-write (see Note 8)	96		105		120		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 10)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 10)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ going low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ going low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ going low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ going high	18		20		25		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ going high	18		20		25		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ going low (early-write operation only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ going low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	15		15		15		ns
t_{DH}	Hold time, data (see Note 12)	15		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 13)	0		0		5		ns

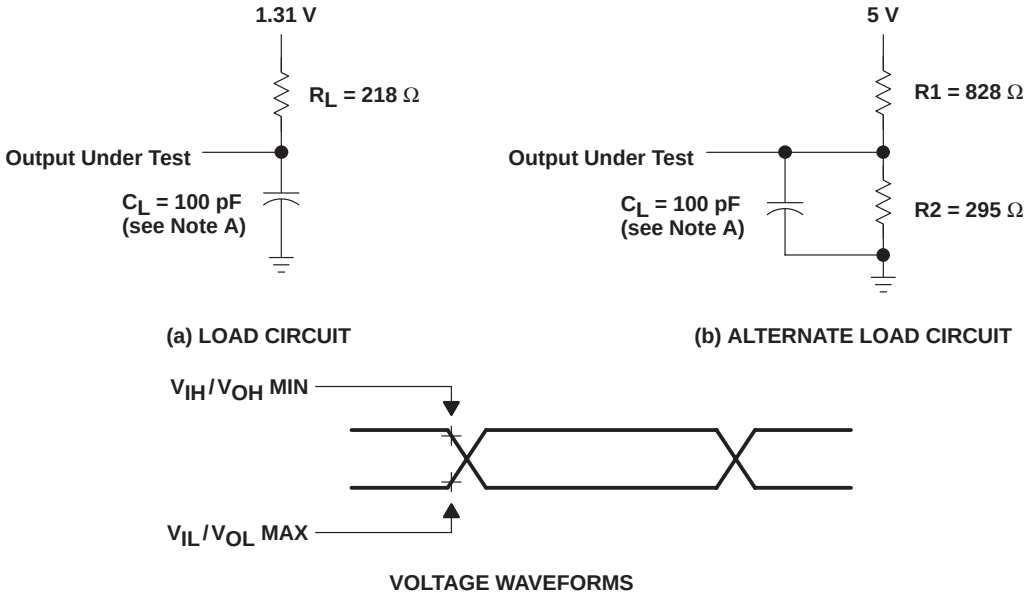
NOTES: 8. All cycle times assume t_T = 5 ns, referenced to $V_{IH(min)}$ and $V_{IL(max)}$.
9. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		’416400-70		’416400-80		’416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	15		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{OEH}	Hold time, $\overline{OE}$ command	18		20		25		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$ low after $\overline{CAS}$ precharge	40		45		50		ns
t_{AWD}	Delay time, column address to $\overline{W}$ going low (read-write operation only)	63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ going high (CBR refresh only)	10		10		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ going low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ going high	70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ going low (CBR refresh only)	5		5		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ going low (read-write operation only)	46		50		60		ns
t_{OED}	Delay time, $\overline{OE}$ to data	18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 14)	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ going high	35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ going high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ going low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ going high	18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ going low (read-write operation only)	98		110		135		ns
t_{CPW}	Delay time, $\overline{W}$ going low after $\overline{CAS}$ precharge (read-write operation only)	63		70		80		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3†	30†	3†	30†	3†	30†	ns

† Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 30 ns. This is assured by design but not tested.
NOTE 14: The maximum value is specified only to assure access time.

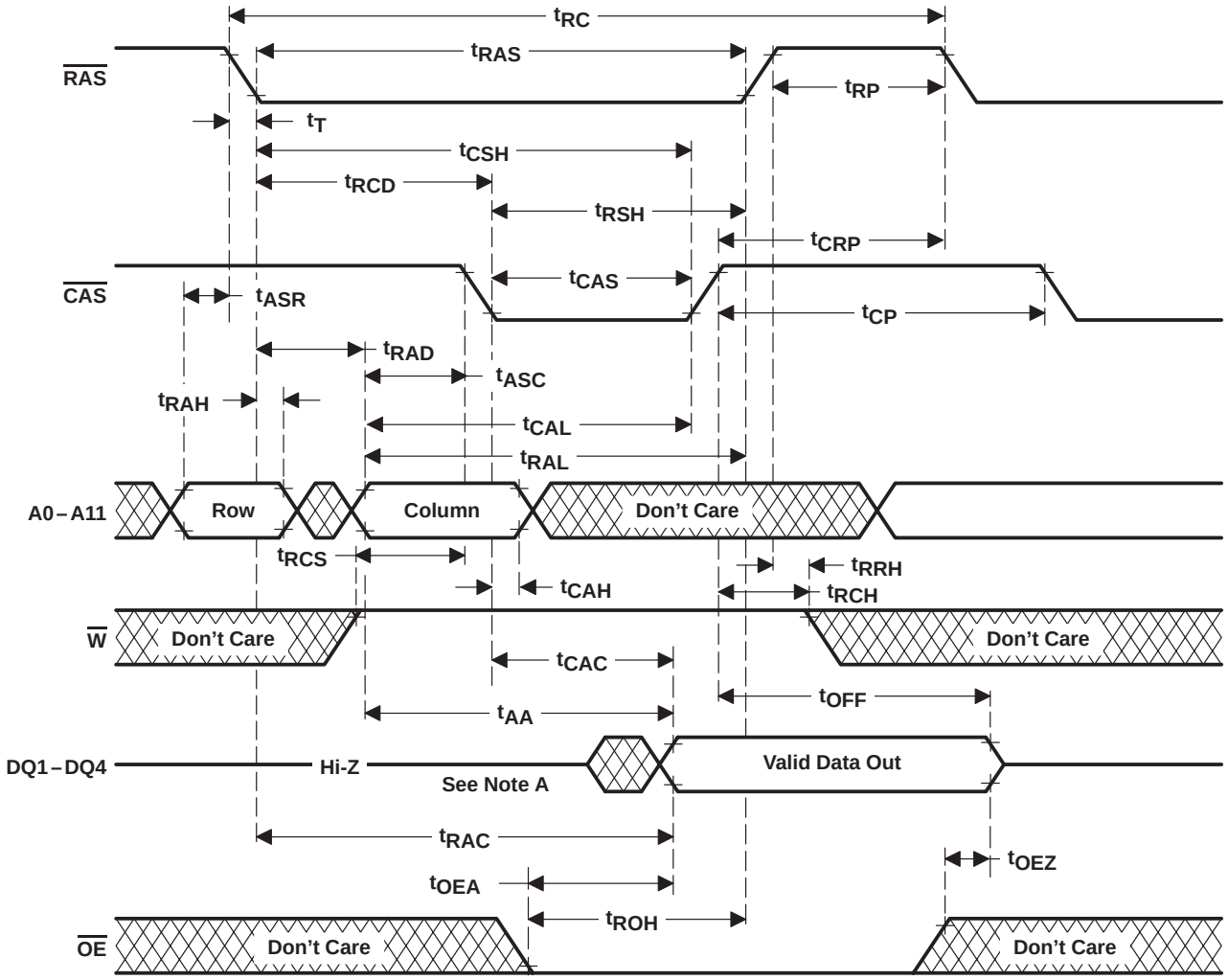
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and fixture capacitance.
B. The ac timing parameters are specified with reference to the minimum valid high-level voltage and the maximum valid low-level voltage for each signal. This corresponds to 2.4 V and 0.8 V for inputs; 2.4 V and 0.4 V for outputs with the given load circuit.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

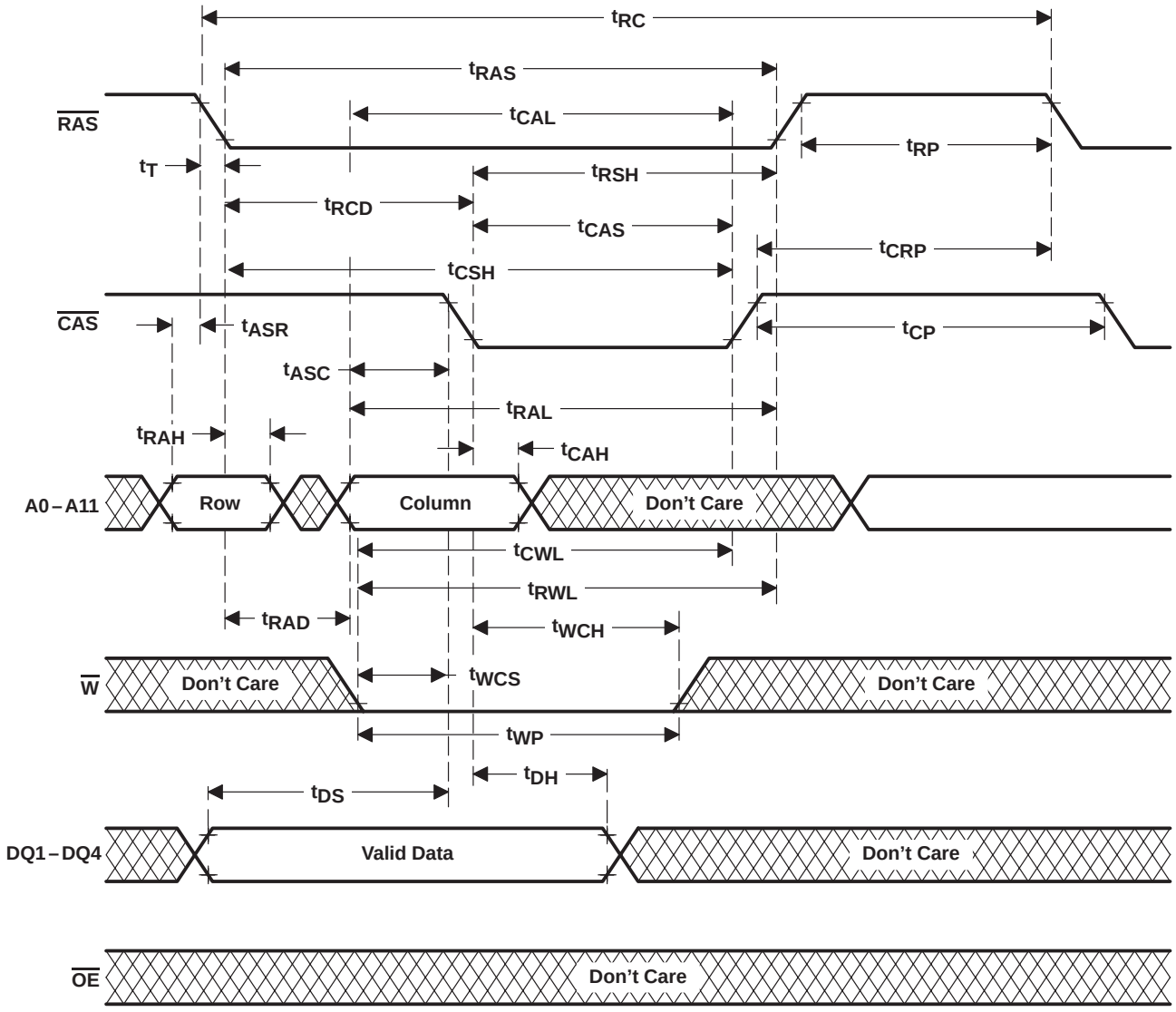


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

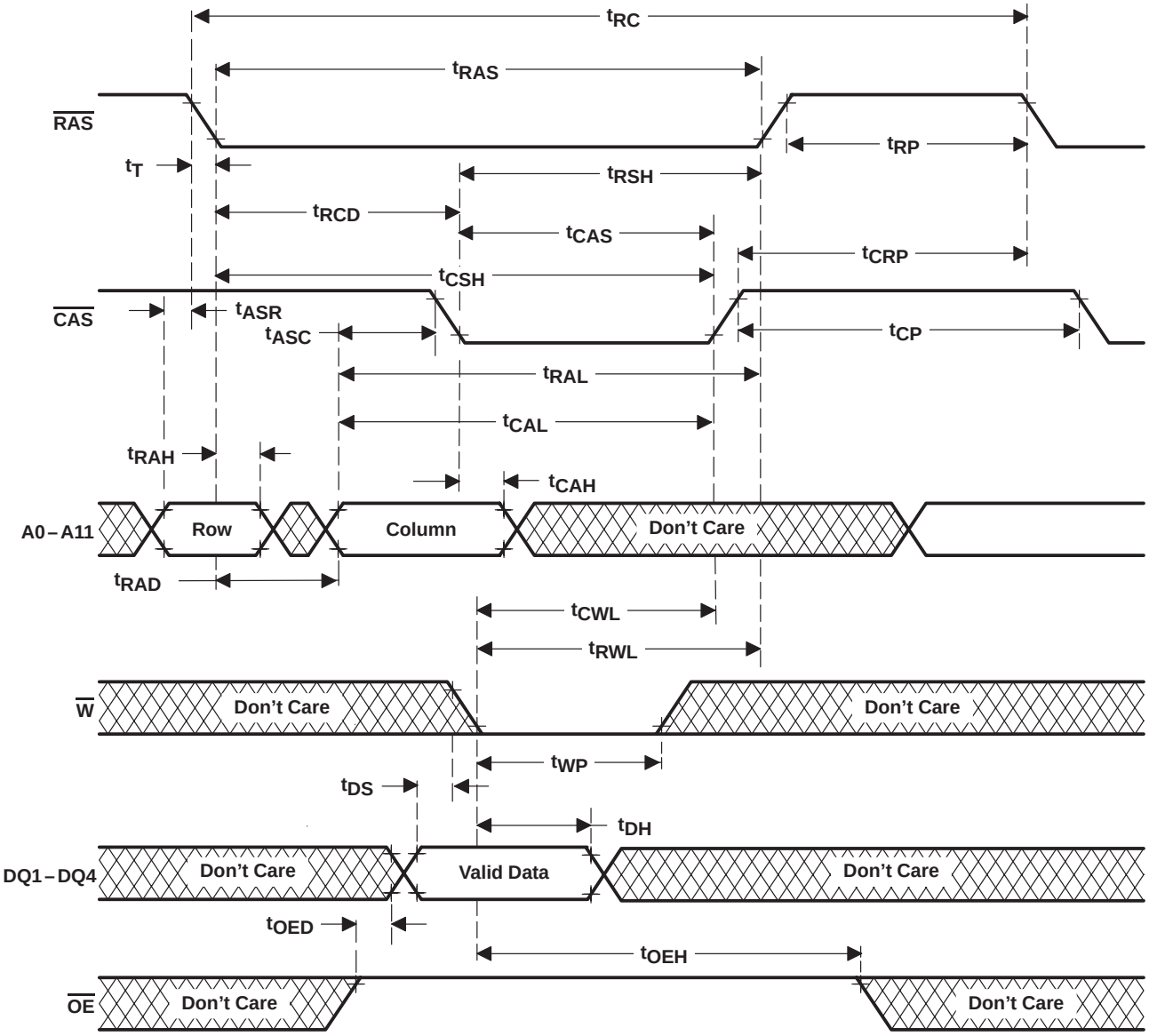
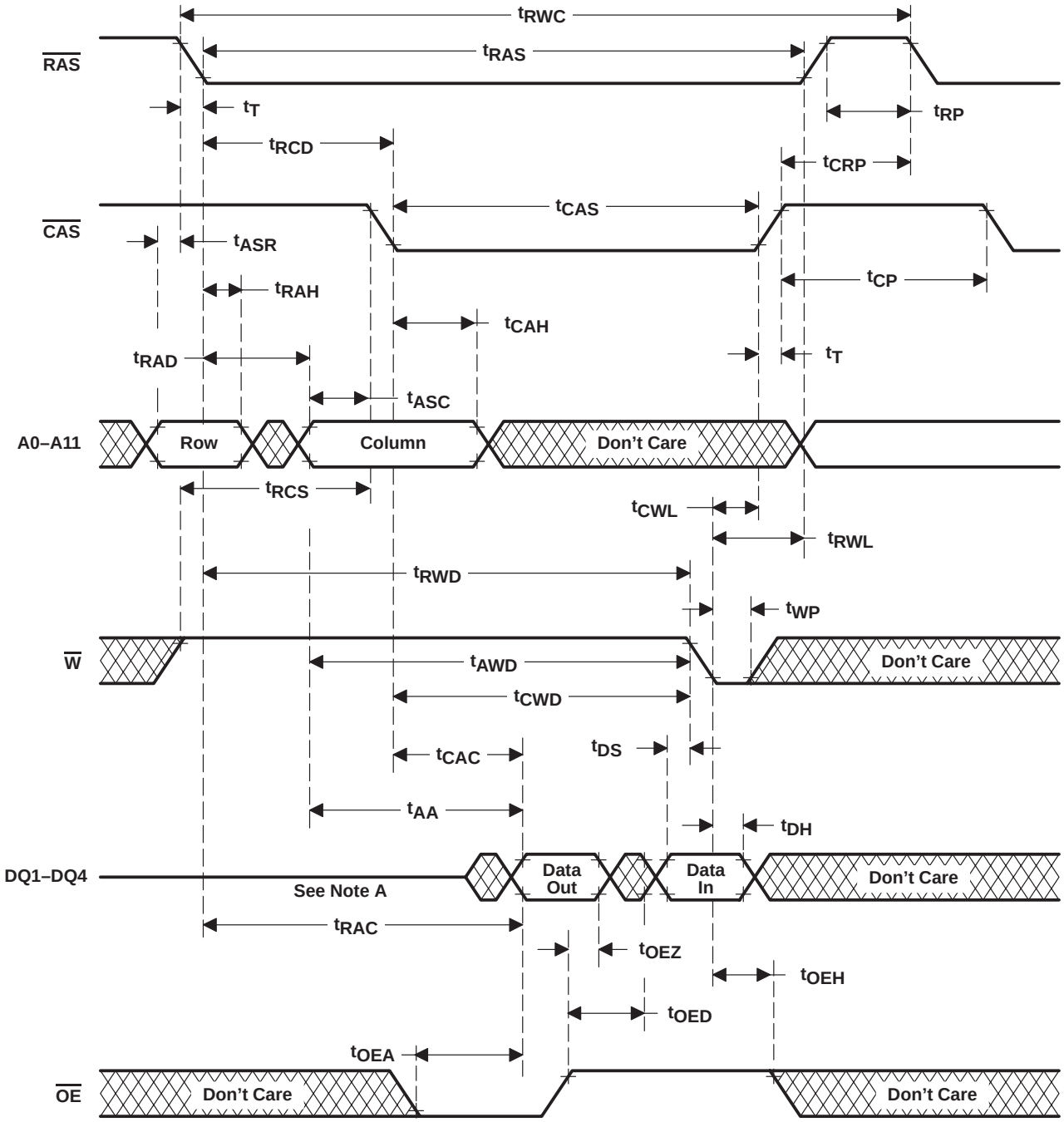


Figure 4. Write-Cycle Timing

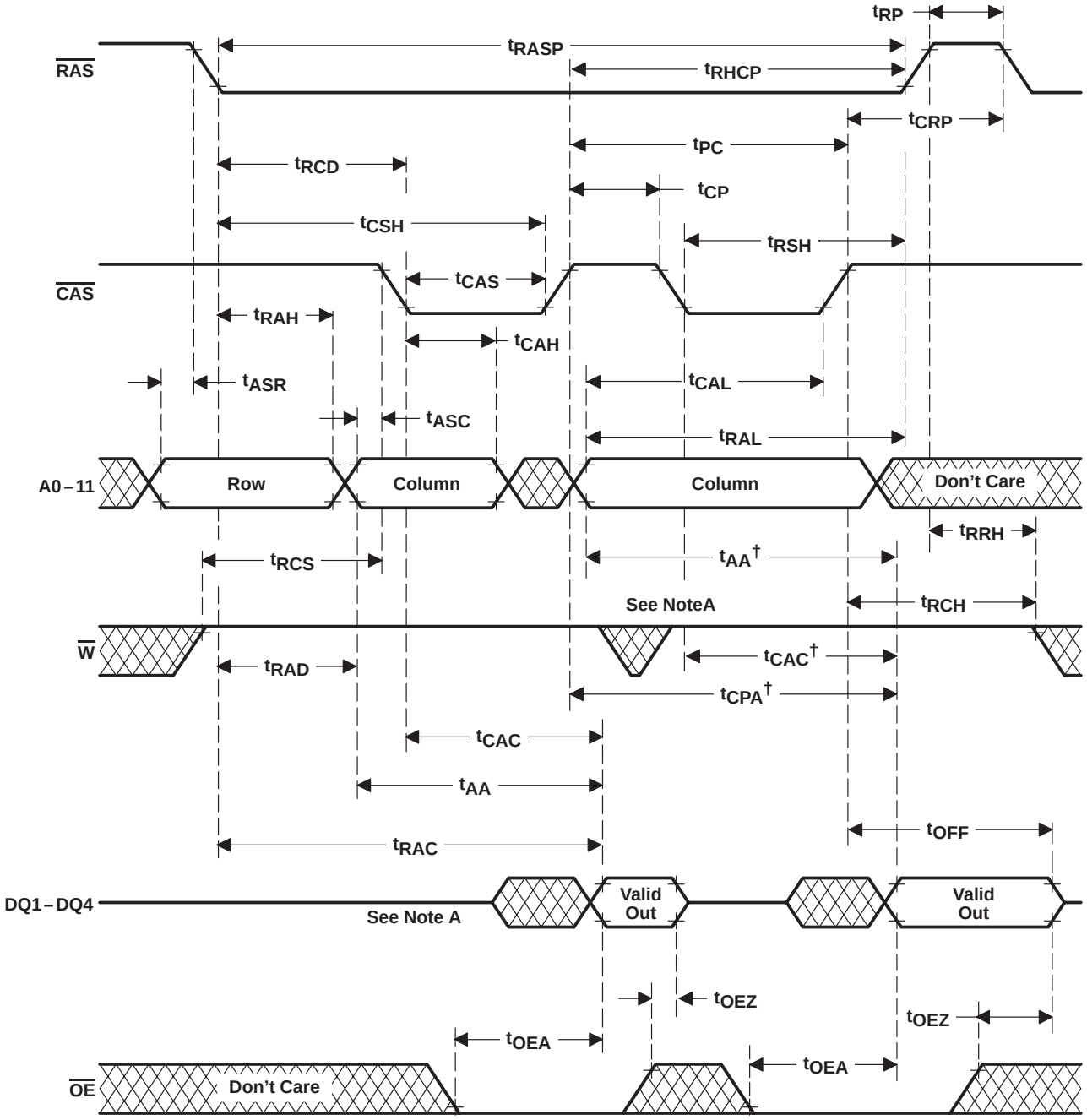
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

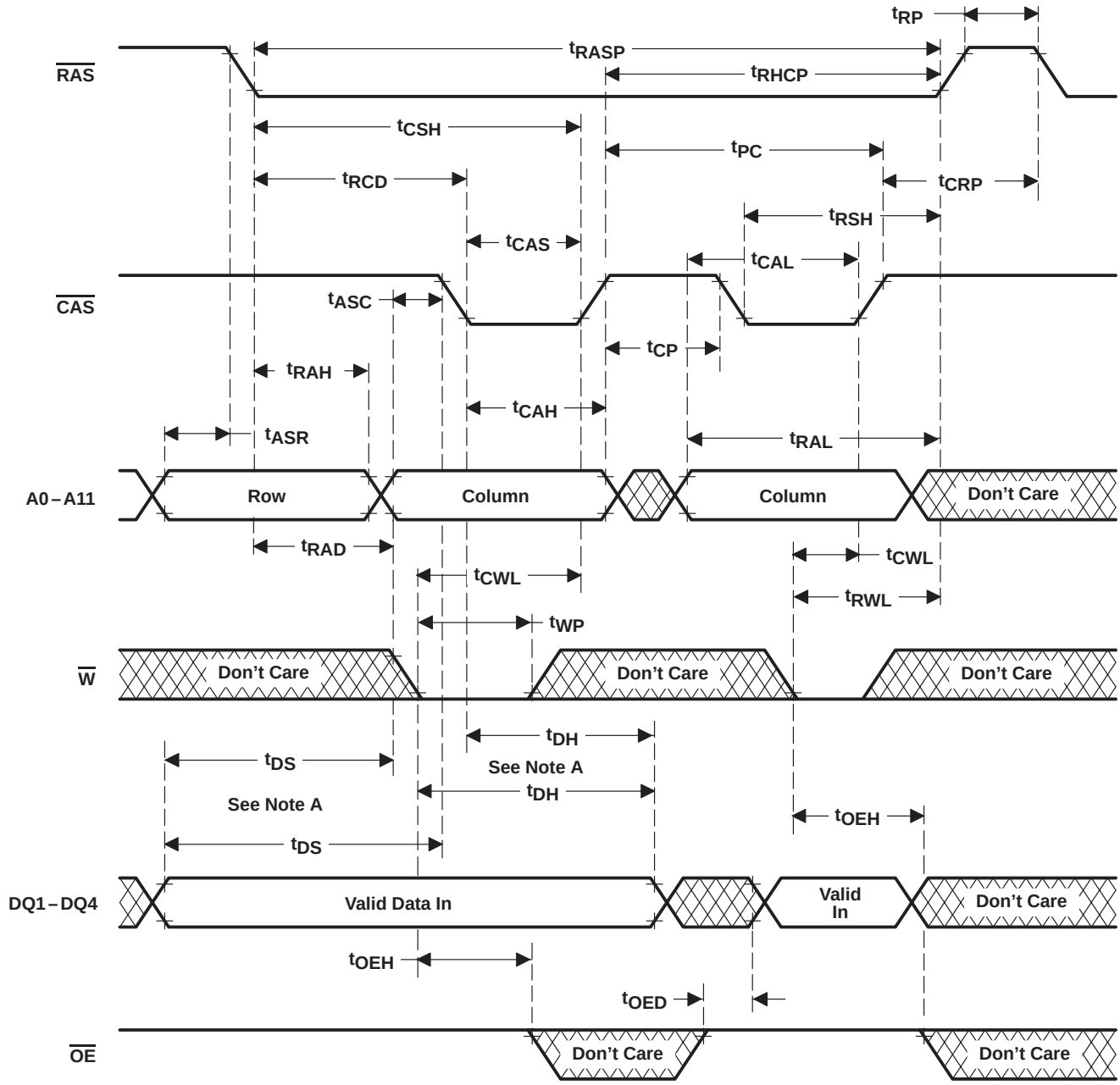
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}-, t_{CAC}- or t_{AA}-dependent.
NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

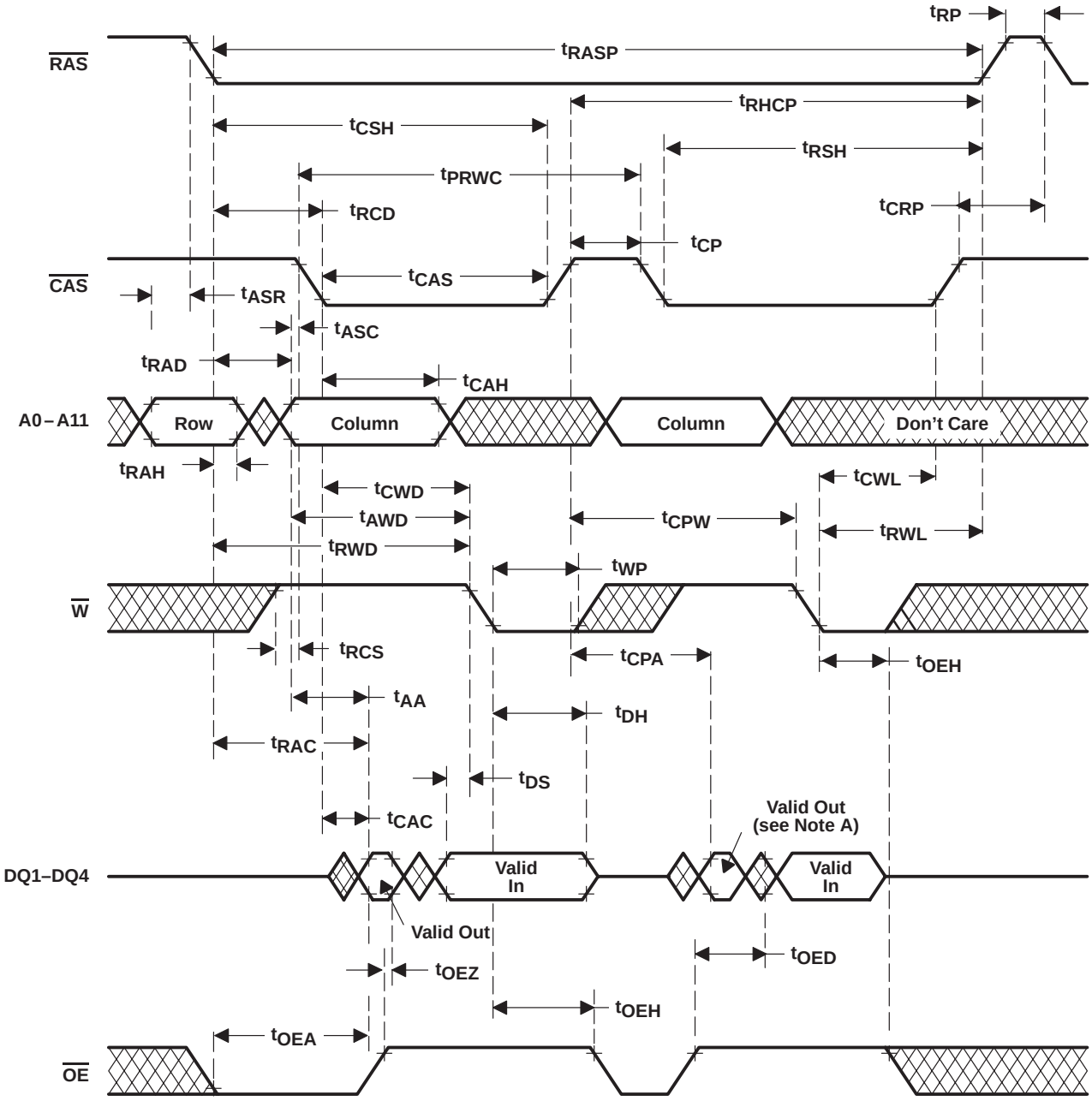
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with a write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

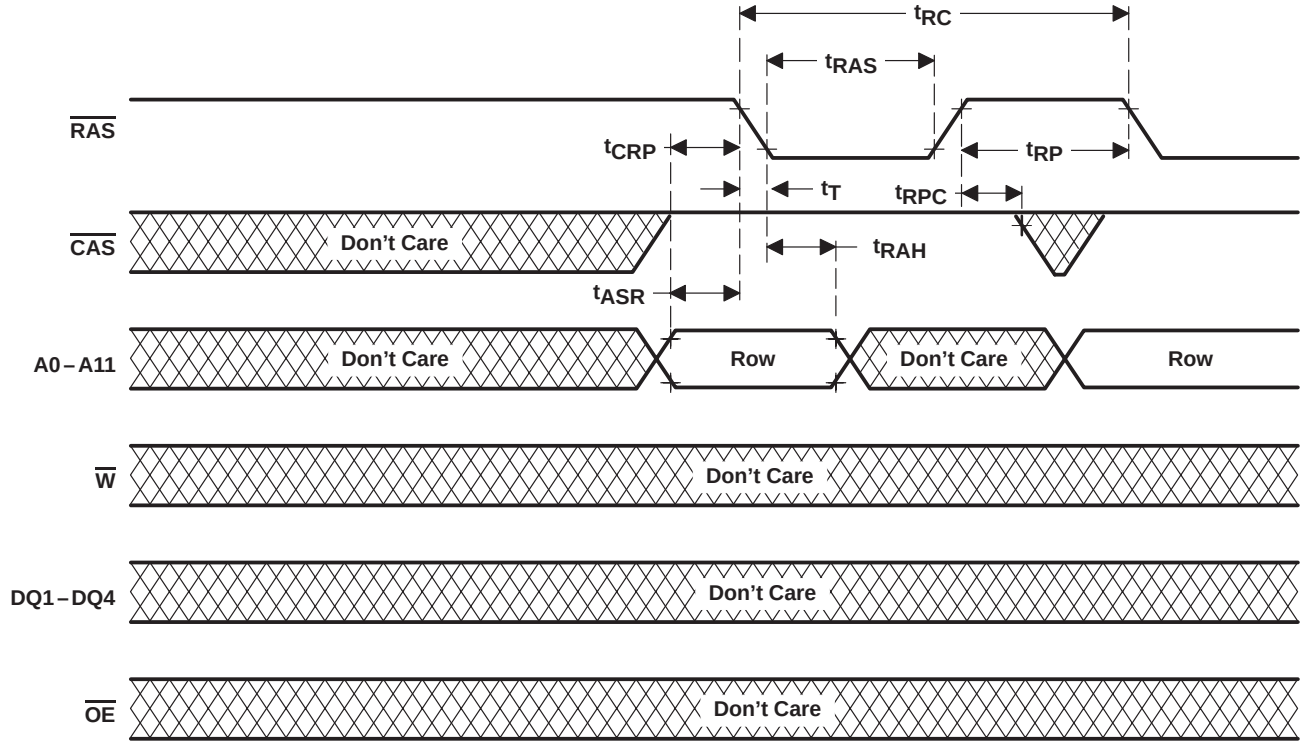


Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

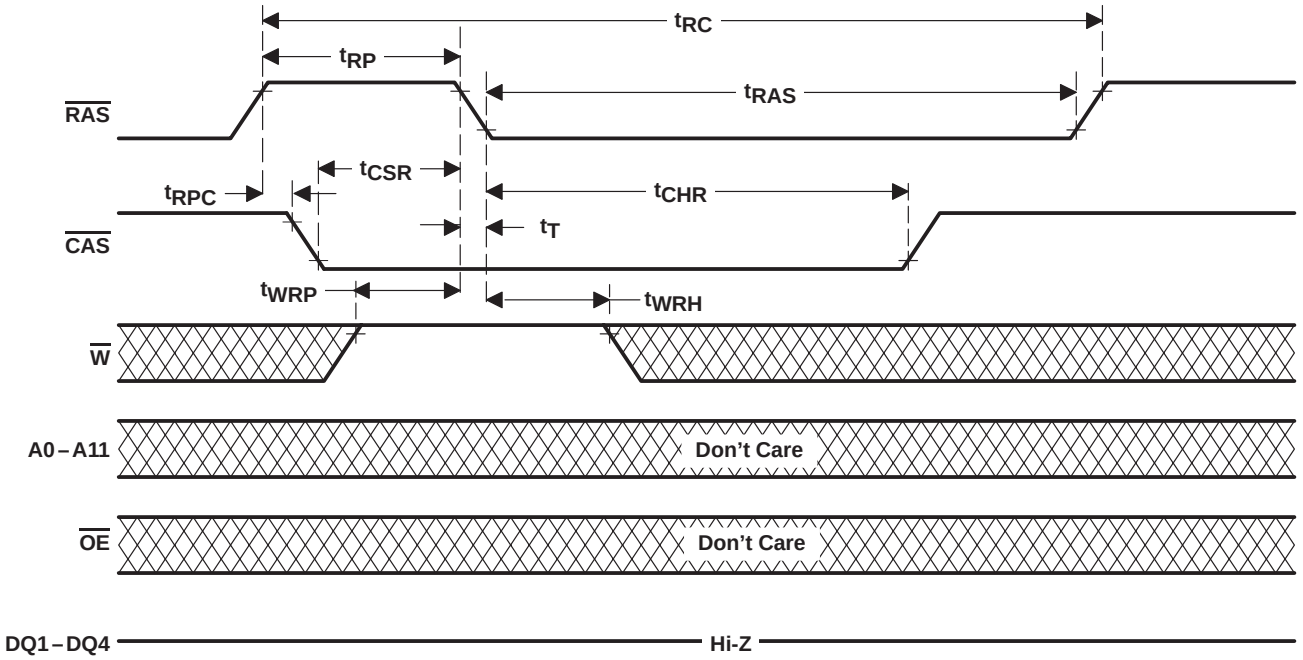


Figure 10. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

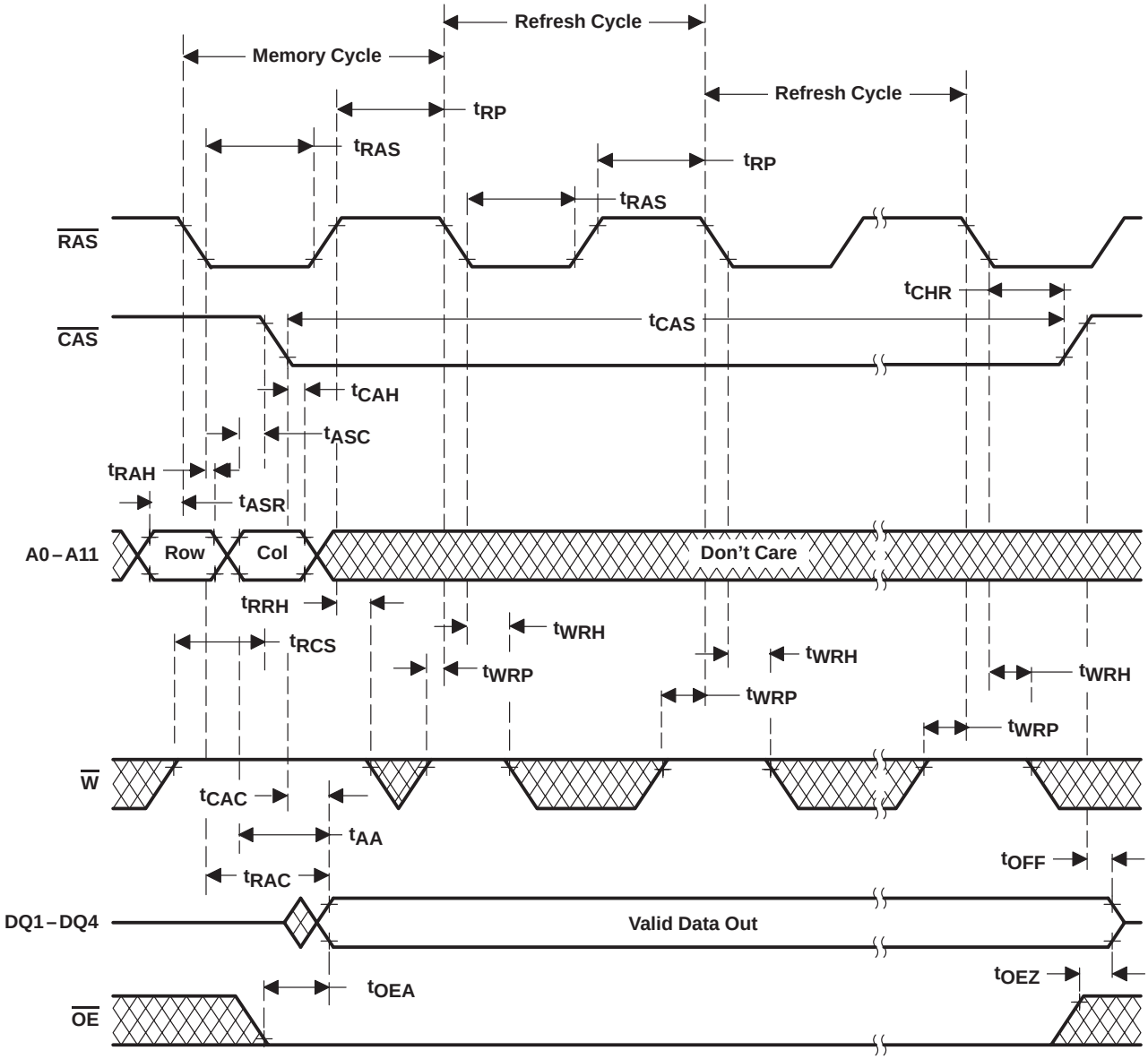


Figure 11. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

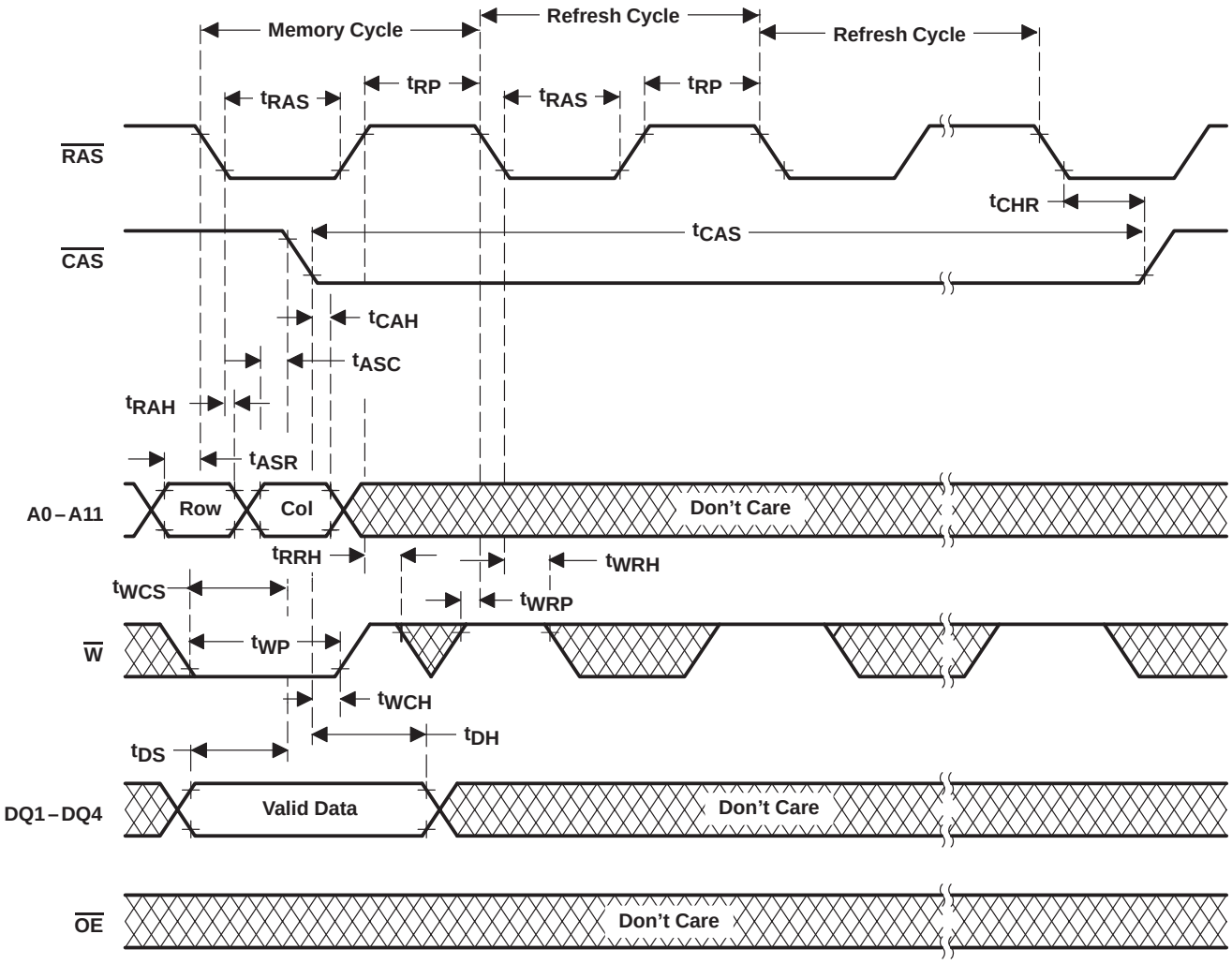
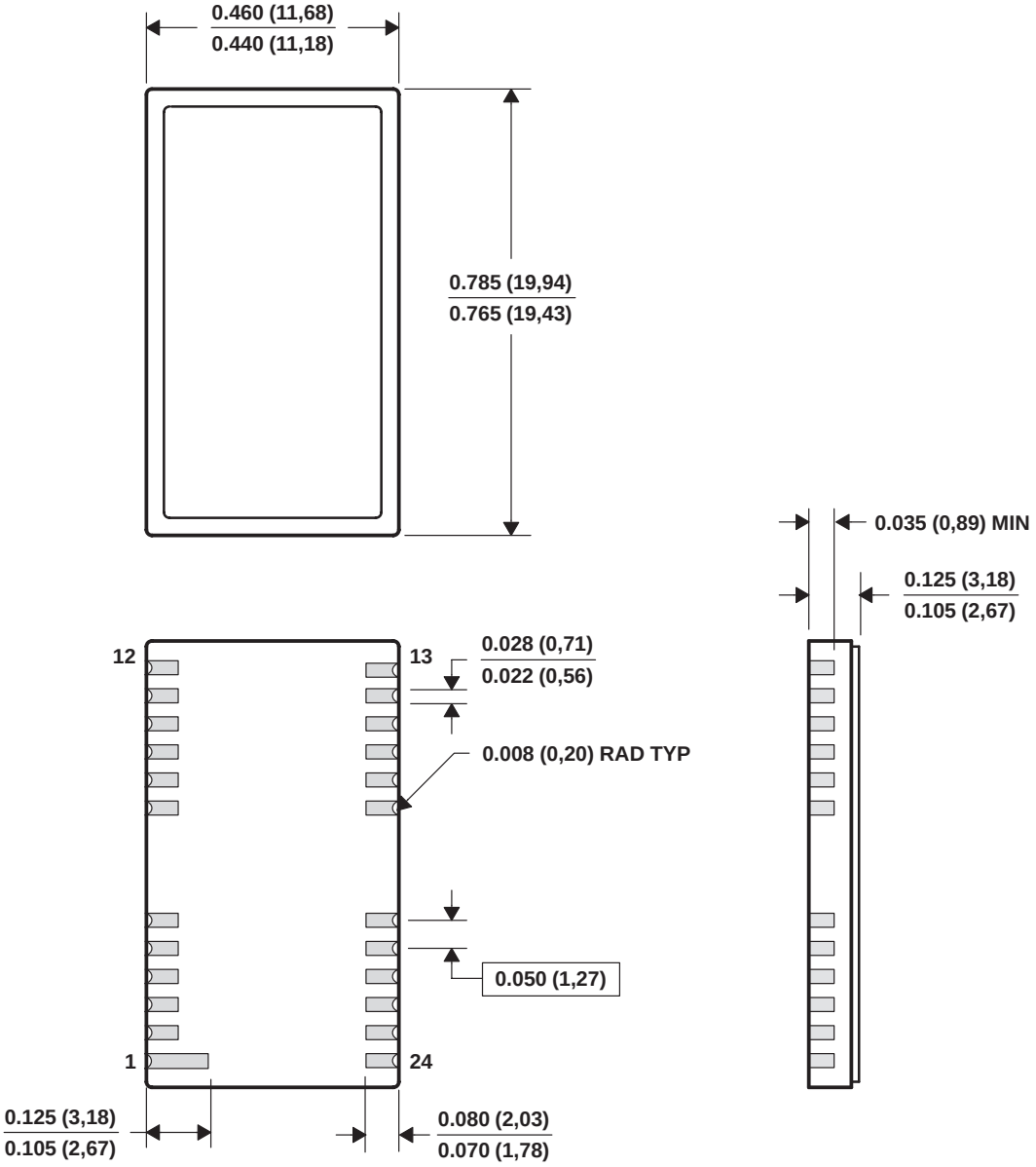


Figure 12. Hidden-Refresh-Cycle (Write) Timing

MECHANICAL DATA

FNC (R-CDCC-N24/28) **LEADLESS CERAMIC CHIP CARRIER**

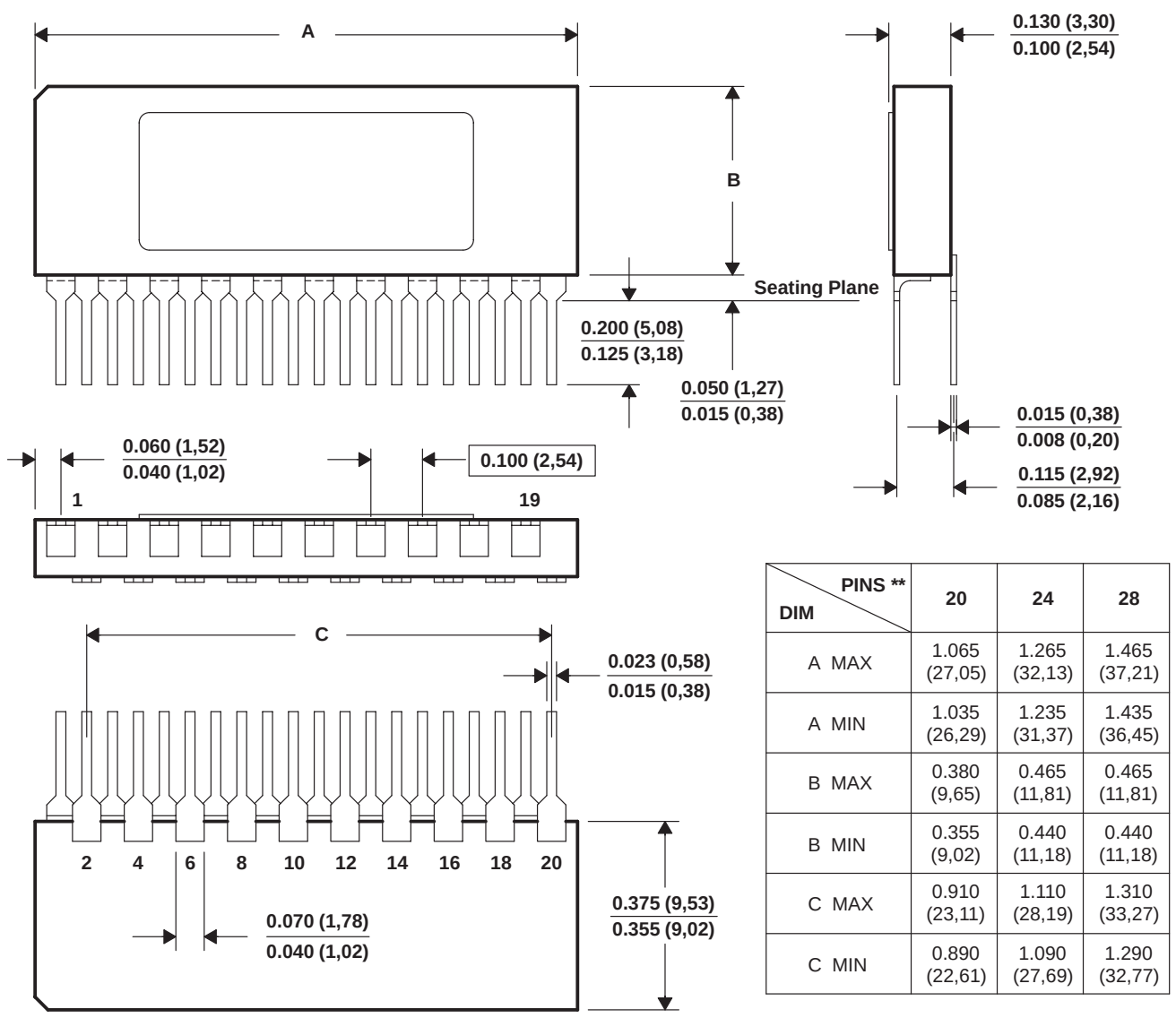


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

MECHANICAL DATA

SV (R-CZIP-T)** **CERAMIC ZIG-ZAG PACKAGE**

20 PIN SHOWN



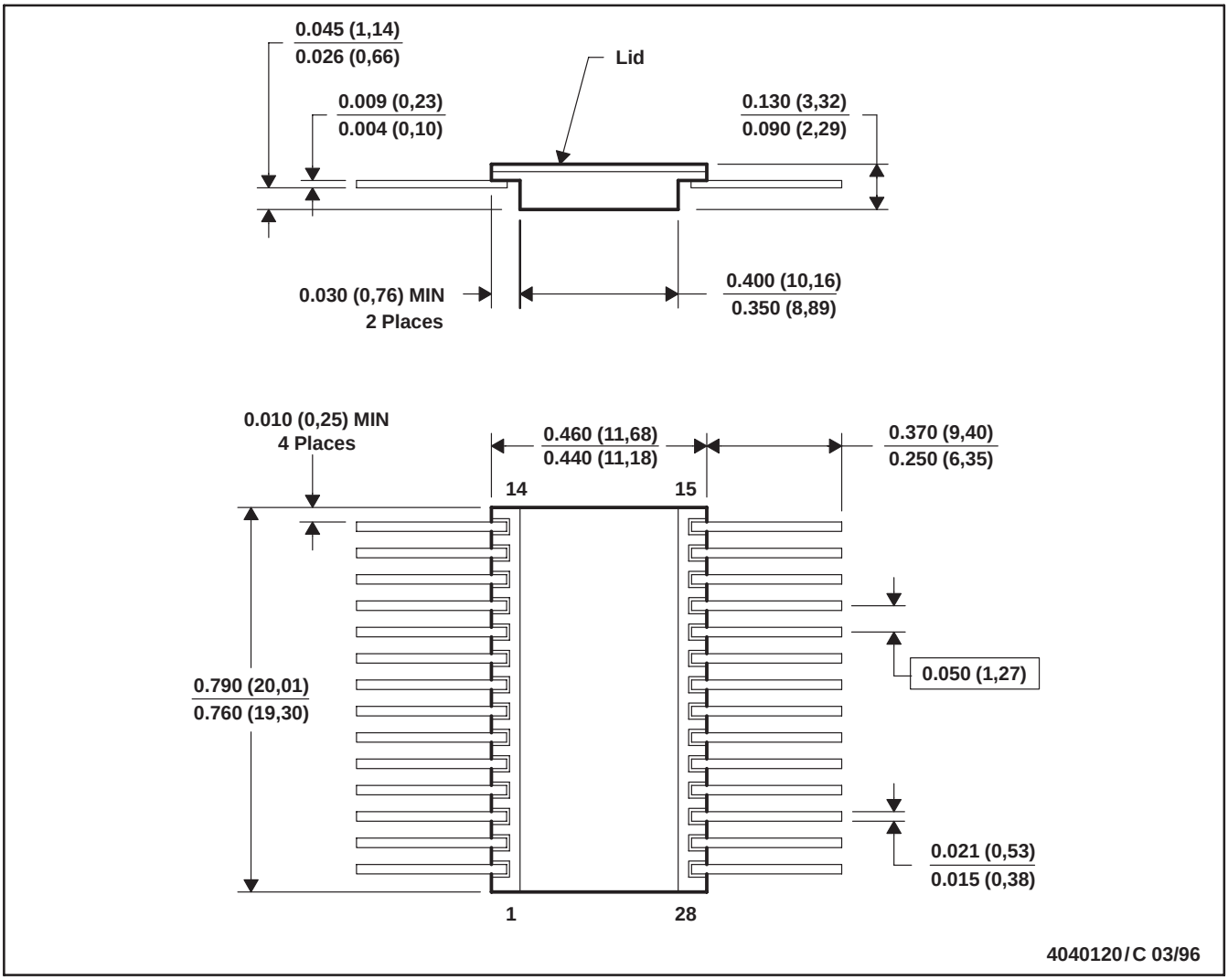
DIM \ PINS **	20	24	28
A MAX	1.065 (27,05)	1.265 (32,13)	1.465 (37,21)
A MIN	1.035 (26,29)	1.235 (31,37)	1.435 (36,45)
B MAX	0.380 (9,65)	0.465 (11,81)	0.465 (11,81)
B MIN	0.355 (9,02)	0.440 (11,18)	0.440 (11,18)
C MAX	0.910 (23,11)	1.110 (28,19)	1.310 (33,27)
C MIN	0.890 (22,61)	1.090 (27,69)	1.290 (32,77)

4040002 / C 08/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

MECHANICAL DATA

HKB (R-CDFP-F28) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

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