

APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ Computer I/O Ports - SCSI, FireWire & USB
- ✓ Set-Top Box Protection
- ✓ Video Card

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20 μ s - Level 2(Line-Gnd) & Level 3(Line-Line)

FEATURES

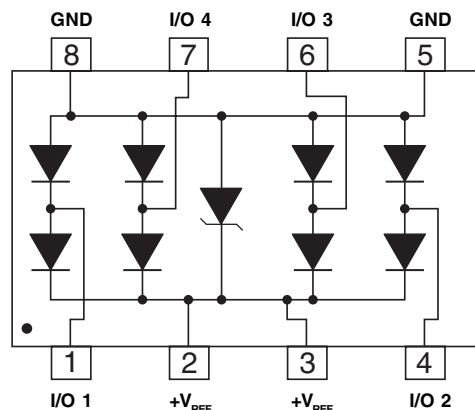
- ✓ 500 Watts Peak Pulse Power per Line (tp=8/20 μ s)
- ✓ Unidirectional Configuration
- ✓ Available in 4 Voltage Types: 3.3V to 15V
- ✓ Protects Up to Four (4) I/O Ports
- ✓ ESD Protection > 40 kilovolts
- ✓ Low Capacitance: 15pF
- ✓ RoHS Compliant

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8
- ✓ Weight 70 milligrams (Approximate)
- ✓ Available in Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
Pure-Tin - Sn, 100: 260-270°C
- ✓ Consult Factory for Leaded Device Availability
- ✓ Flammability Rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code, Logo, Date Code & Pin One Defined By Dot on Top of Package


SO-8

PIN CONFIGURATION



PSRDA3.3-4 thru PSRDA15-4

DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	500	Watts
Operating Temperature	T_L	-55 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Maximum Forward Voltage @ 100mA (See Note 1)	V_F	1.1	Volts

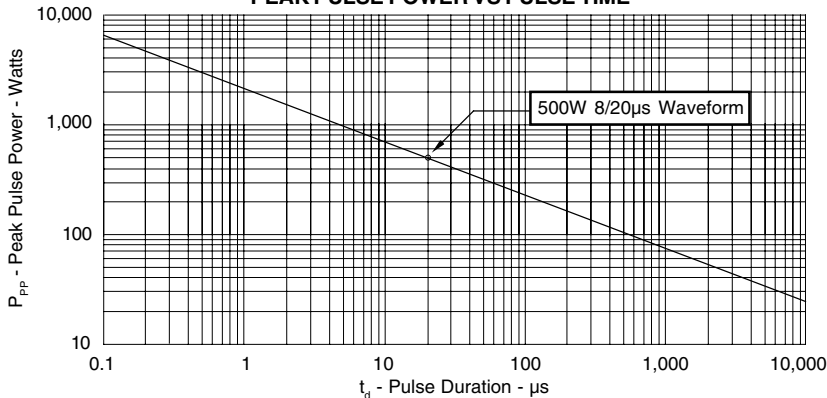
Note 1: Measured between pins 8 or 5 to 1, 2, 3, 4, 6 and 7.

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified

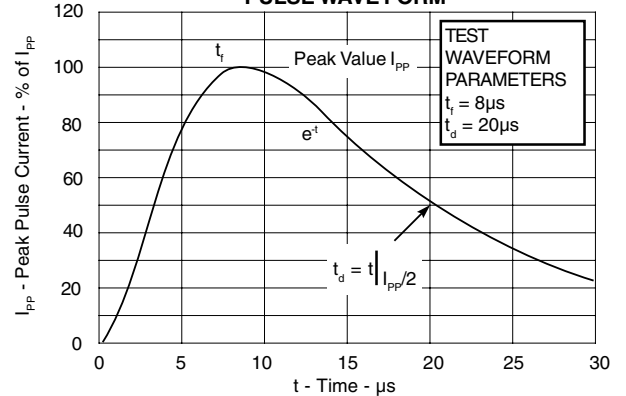
PART NUMBER	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ $I_P = 1A$ V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20 μs $V_C @ I_{PP}$	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D μA	MAXIMUM CAPACITANCE (See Note 1) (See Figure 5) @ 0V, 1 MHz $C_{i(SD)}$ pF
PSRDA3.3-4	PRA	3.3	4.0	6.5	10.9V @ 43.0A	125	15
PSRDA05-4	PRB	5.0	6.0	9.8	13.5V @ 42.0A	20	15
PSRDA12-4	PRD	12.0	13.3	19.0	25.9V @ 21.0A	1	15
PSRDA15-4	PRE	15.0	16.7	24.0	30.0V @ 17.0A	1	15

Note 1: Capacitance measured at $V_{WM} = V_{CC}$ connected between I/O pins to pin 8 and 5 (Gnd). $V_R = V_{WM}$ @ 1MHz. As shown in Figure 5, REF1 is connected to ground, REF2 is connected to $+V_{CC}$, and input applies to $V_{CC} = 5V$, $V_{sign} = mV$, $F = 1$ MHz.

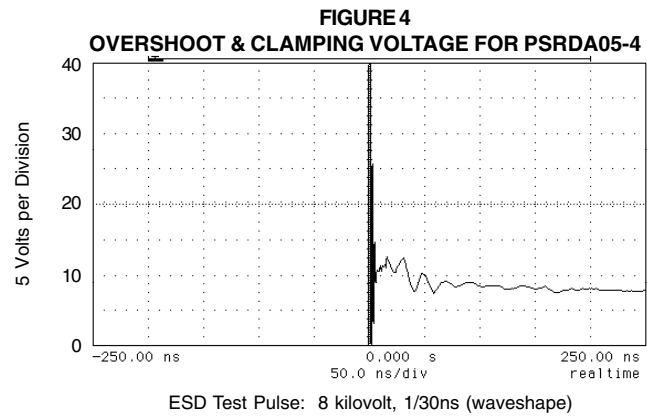
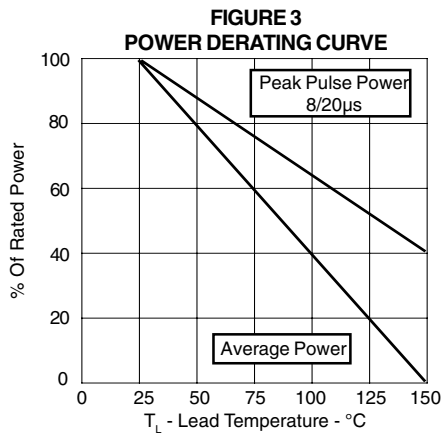
**FIGURE 1
PEAK PULSE POWER VS PULSE TIME**



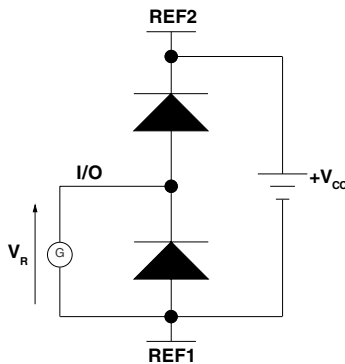
**FIGURE 2
PULSE WAVE FORM**



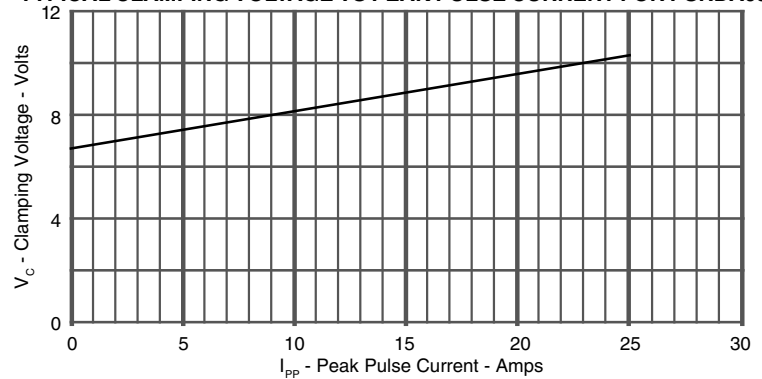
GRAPHS



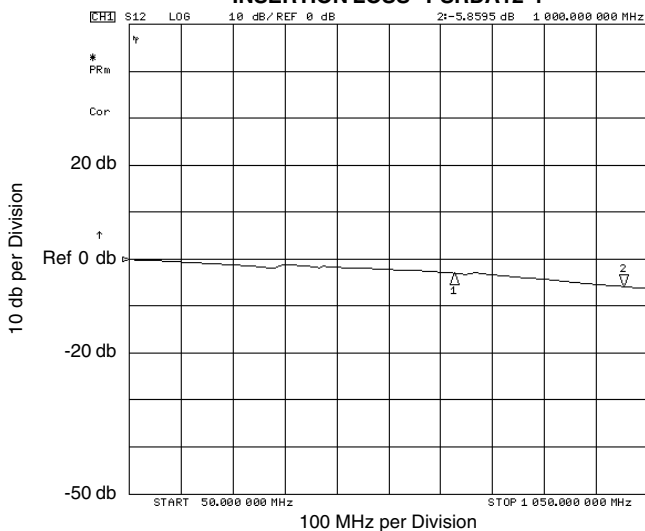
**FIGURE 5
INPUT CAPACITANCE CIRCUIT**



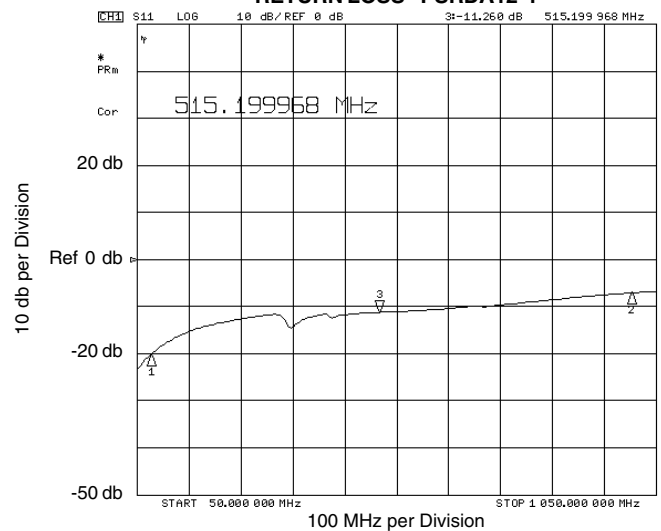
**FIGURE 6
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR PSRDA05-4**



**FIGURE 7
INSERTION LOSS - PSRDA12-4**



**FIGURE 8
RETURN LOSS - PSRDA12-4**



APPLICATION NOTE

The PSRDAxx-4 Series are low capacitance, unidirectional TVS arrays that are designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product series has a surge capability of 500 Watts P_{PP} per line for an 8/20 μ s waveshape and offers ESD protection > 40kV.

DIFFERENTIAL-MODE CONFIGURATION (Figure 1)

Ideal for use in USB applications, the PSRDAxx-4 Series provides up to four (4) lines of protection in a differential-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Pins 1, 4, 6 and 7 are connected to the data lines.
- ✓ Pins 5 and 8 are connected to ground.
- ✓ Pins 2 and 3 are connected to the databus.

DIFFERENTIAL-MODE CONFIGURATION (Figure 2)

The PSRDAxx-4 Series also provides up to four (4) lines of protection in a differential-mode configuration as depicted in Figure 2 for T1/E1 applications.

Circuit connectivity is as follows:

- ✓ Pins 1, 4, 6 and 7 are connected to the data lines.
- ✓ Pins 5 and 8 are connected to ground.
- ✓ Pins 2 and 3 are connected to the databus.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1. Typical Differential-Mode USB Protection

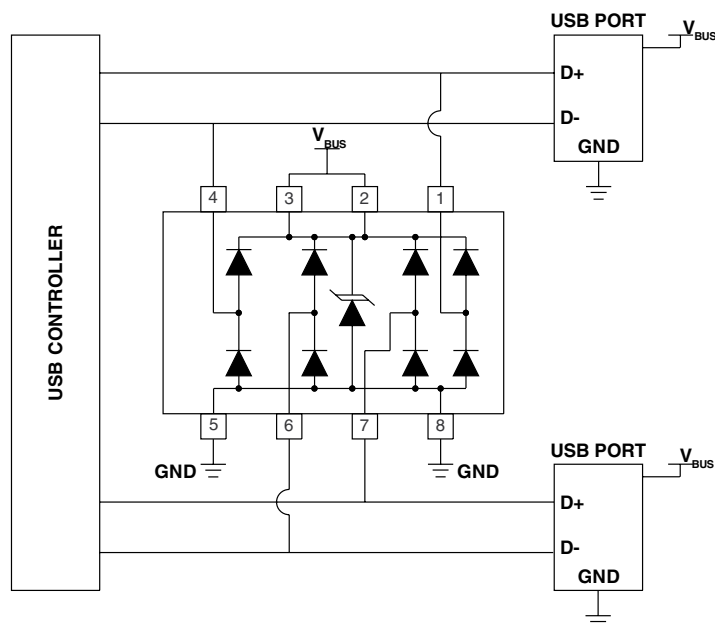
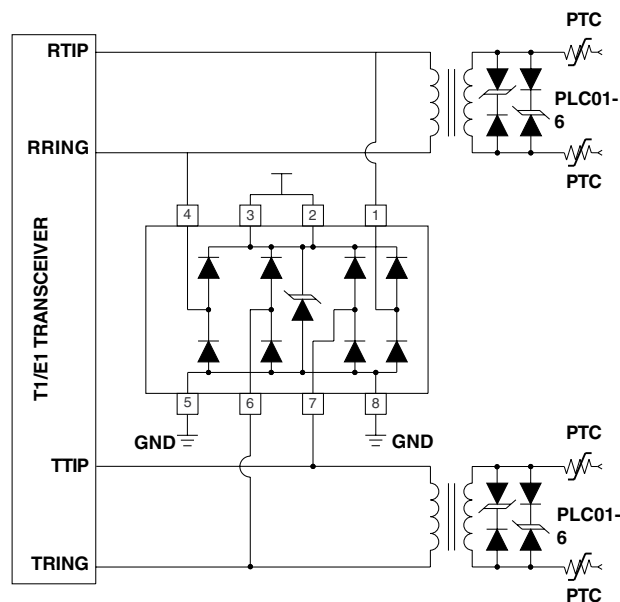
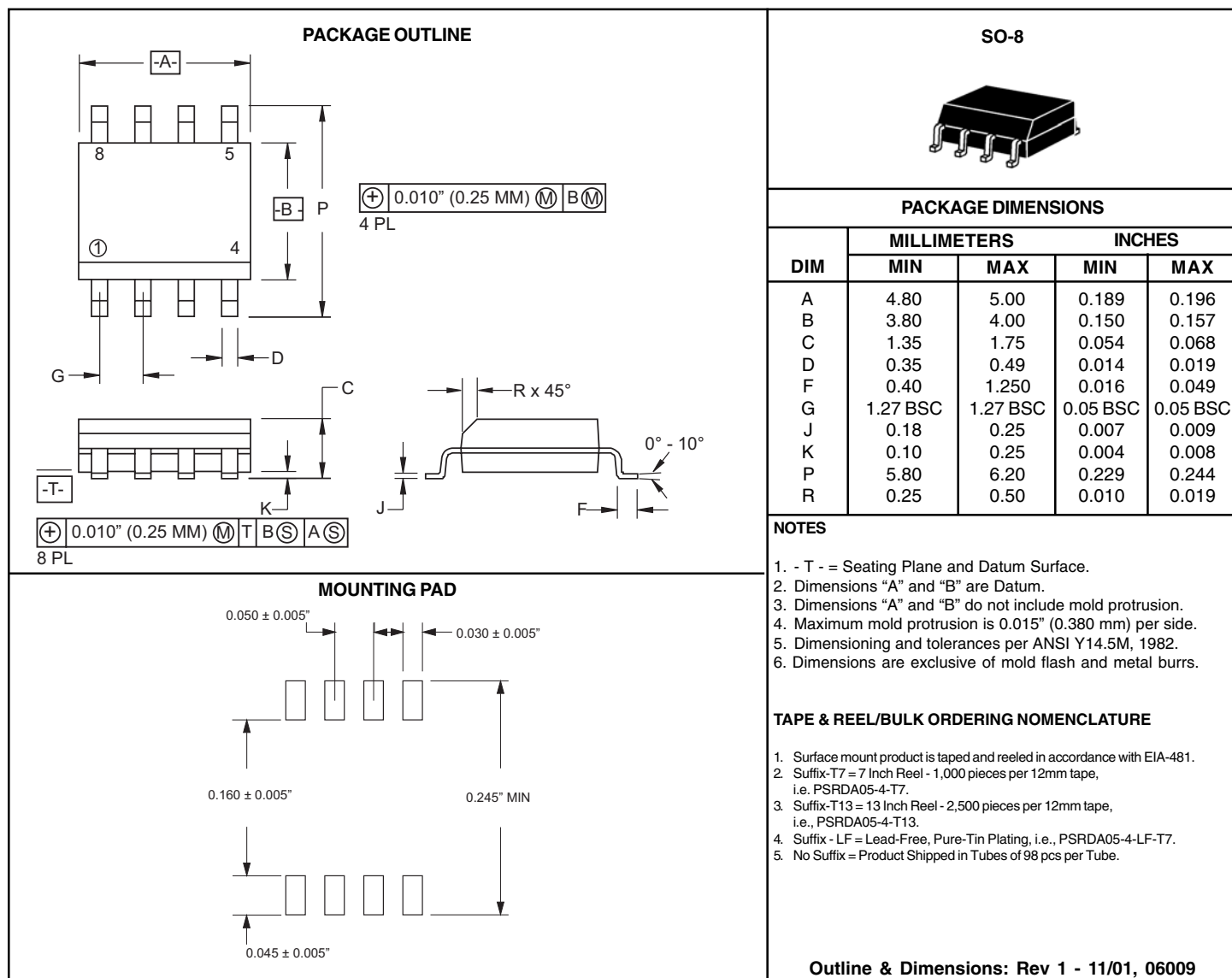


Figure 2. Typical Differential-Mode T1/E1 Protection



PSRDA3.3-4 thru PSRDA15-4

SO-8 PACKAGE OUTLINE & DIMENSIONS



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