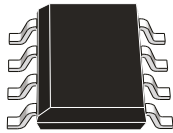# High voltage, precision, bidirectional current sense amplifier

SO8

MiniSO8

Features

- Wide common mode voltage: - 20 to 70 V
- Offset voltage: ± 200 µV max.
- 2.7 to 5.5 V supply voltage
- Gain: 60 V/V
- Gain error: 0.3% max.
- Offset drift: 5 µV/°C max.
- Gain drift: 10 ppm/°C max.
- Quiescent current: 20 µA in shutdown mode
- SO8 and MiniSO8 package

Applications

- High-side current sensing
- Low-side current sensing
- Data acquisition and instrumentation
- Test and measurement equipment
- Industrial process control
- Motor control
- Solenoid control

Maturity status link
TSC2011

Description

The TSC2011 is a precision bidirectional current sense amplifier. It can sense the current thanks to a shunt resistor over a wide range of common mode voltages, from - 20 to + 70 V, whatever the supply voltage is. It is available with an amplifier gain of 60 V/V.
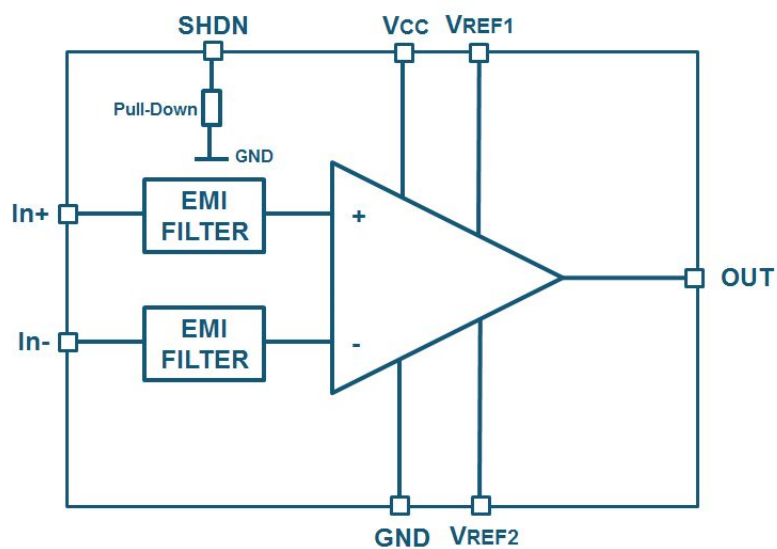
It is able to sense very low drop voltages as low as 10 mV full scale minimizing the measurement error.

The TSC2011 can also be used in other functions such as: precision current measurement, overcurrent protection, current monitoring, and feedback loops.

This device fully operates over the broad supply voltage range from 2.7 to 5.5 V and over the industrial temperature range from -40 to 125 °C.

DS13057 - Rev 1 - September 2019
For further information contact your local STMicroelectronics sales office.

www.st.com

1 Diagram

Figure 1. Block diagram

2 Pin configuration

Figure 2. Pin connection (top view)

Table 1. Pin description

Pin	Pin name	Description
1	IN -	Negative input
2	GND	Ground
3	VREF2	Reference voltage 2
4	SHDN	Shutdown
5	OUT	Output
6	VCC	Supply voltage
7	VREF1	Reference voltage 1
8	IN +	Positive input

3   Maximum ratings

Table 2. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	-0.3 to 7	V
V_{ICM}	Common mode voltage on input pins	-25 to 76	V
V_{DIF}	Differential voltage between input pins (In+, In-)	7	V
V_{REF1} V_{REF2} V_{OUT}	Voltage present on pins Ref1, Ref2, Out	Gnd - 0.3 to V_{cc} + 0.3	V
I_{IN}	Input current to any pins [2]	5	mA
T_{STG}	Storage temperature	-65 to 150	°C
T_J	Junction temperature	150	°C
R_{THJA}	Thermal resistance junction to ambient [3][4] SO8 MiniSO8	 125 190	°C/W
ESD	Human body model (HBM) [5]	2000	V
	Charged device model (CDM) [6]	1000	
	Latch-up immunity	200	mA

1. *All voltage values, except the differential voltage are with respect to the network ground terminal.*
2. *Input voltage can go beyond supply voltage but input current must be limited. Using a serial resistor with the input is highly recommended in that case.*
3. *Short-circuits can cause excessive heating and destructive dissipation.*
4. *R_{th} are typical values.*
5. *According to JEDEC standard JESD22-A114F.*
6. *According to ANSI/ESD STM5.3.1.According to ANSI/ESD STM5.3.1.*

Table 3. **Operating conditions**

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	2.7 to 5.5	V
V_{icm}	Common mode voltage on input pins	-20 to +70	V
V_{ref}	Output offset adjustment range	0 to V_{cc}	V
T	Operating free-air temperature range	-40 to 125	°C

4 Electrical characteristics

Table 4. Electrical characteristics V_{cc} = 2.7 V, V_{icm} = 12 V, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
I_{cc}	Current consumption	V_{icm} = -20 to 70 V		1.5	2.3	mA
		$T_{min} < T < T_{max}$			2.3	
	Current consumption with shutdown active	V_{icm} = - 20 to 70 V		20	50	µA
		$T_{min} < T < T_{max}$			150	
Input						
$\lvert V_{os} \rvert$	Offset voltage (RTI) [1]	V_{icm} = 1 V			200	µV
		$T_{min} < T < T_{max}$			700	
		V_{icm} = 12 V			500	
		$T_{min} < T < T_{max}$			1100	
$\lvert \Delta V_{os}/\Delta T \rvert$	Offset drift vs. temperature	V_{icm} = 1 V, $T_{min} < T < T_{max}$			5	µV/°C
		V_{icm} = 12 V, $T_{min} < T < T_{max}$			8	
CMR	Common mode rejection	V_{icm} = -20 to 70 V, DC mode	95	115		dB
		$T_{min} < T < T_{max}$	90			
I_{ib+}	Input bias current	V_{icm} = 12 V		350		µA
		$T_{min} < T < T_{max}$, V_{icm} = -20 to 70 V	-400		600	
I_{ib-}	Input bias current	V_{icm} = 12 V		100		
		$T_{min} < T < T_{max}$, V_{icm}= - 20 to 70 V	-150		350	
$\lvert V_{sense} \rvert$	Vsense operating range with Eg ≤ 0.3% [2]	TSC2011			40.5	mV
		$T_{min} < T < T_{max}$			39.3	
Output						
G	Gain	TSC2011		60		V/V
Eg	Gain error vs. temperature	ΔV_{out} = 100 mV to (V_{cc} - 100 mV)			0.3	%
		$T_{min} < T < T_{max}$			0.3	
$\Delta Eg/\Delta T$	Gain error drift	$T_{min} < T < T_{max}$			10	ppm/°C
NLE	Linearity error	V_{icm} = 12 V		0.03		%
$V_{cc} - V_{oh}$	Drop voltage output high	I_{source} = 0.2 mA		8	15	mV
		$T_{min} < T < T_{max}$			20	
V_{ol}	Output voltage low	I_{sink} = 0.2 mA		12	20	mV
		$T_{min} < T < T_{max}$			30	
I_{out}	Output current	Sink mode		20	40	mA
		$T_{min} < T < T_{max}$			35	
		Source mode	6	10		
		$T_{min} < T < T_{max}$	4			
Reg Load	Load regulation	I_{out} = - 10 to +4 mA		0.3	1.5	mV/mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET adjustment						
R_t	Ratiometric accuracy			0.5		V/V
Acc	Accuracy, RTO	Voltage applied to Vref1 and Vref2 in parallel		0.1		%
Dynamic performances						
BW	Small signal -3 dB bandwidth	$R_l = 10$ kΩ, $C_l = 100$ pF	500	620		kHz
		$T_{min} < T < T_{max}$	250			
SR	Slew rate	$R_l = 10$ kΩ, $C_l = 100$ pF, $V_{icm} = 1$ V	2.7	3.5		V/µs
		$T_{min} < T < T_{max}$	2.5			
E_n	Noise, RTI	0.1 Hz to 10 Hz		37		µVpp
	Spectral density, RTI	f = 1 kHz		100		nV/√Hz
Shutdown function (active high)						
V_{il}	Logical low level		0		$0.3xV_{cc}$	V
V_{ih}	Logical high level		$0.7xV_{cc}$		V_{cc}	
I_{ih}	Leakage current	$V_{shdn} = V_{cc}$ (Shutdown mode)		0.9		µA
T_{on}	Turn-On time	V_{shdn}= 2.7 V to 0 V, $R_l = 10$ kΩ		6		µs
T_{off}	Turn-off time	$V_{shdn} = 0$ V to 2.7 V, R_l= 10 kΩ		3		µs
I_{out}	Output leakage current	Shdn active		50		nA

1. *RTI stands for "Related to input".*

2. $V_{sense}=(V_{in+}) - (V_{in-})$.

Table 5. Electrical characteristics (V$_{cc}$ = 5 V, V$_{icm}$ = 12 V, T = 25 °C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
I$_{cc}$	Current consumption	V$_{icm}$ = -20 to 70 V		1.6	2.4	mA
		T$_{min}$ < T < T$_{max}$			2.4	
	Current consumption with shutdown active	V$_{icm}$ = - 20 to 70 V		20	50	µA
		T$_{min}$ < T < T$_{max}$			150	
SVR	Supply voltage rejection	V$_{cc}$ = 2.7 to 5.5 V	80	100		dB
		T$_{min}$ < T < T$_{max}$	75			
Input						
|V$_{os}$|	Offset voltage (RTI) [1]	V$_{icm}$ = 1 V			200	µV
		T$_{min}$ < T < T$_{max}$			700	
		V$_{icm}$ = 12 V			500	
		T$_{min}$ < T < T$_{max}$			1100	
|ΔV$_{os}$/ΔT|	Offset drift vs. temperature	V$_{icm}$ = 1 V, T$_{min}$ < T < T$_{max}$			5	µV/°C
		V$_{icm}$ = 12 V, T$_{min}$ < T < T$_{max}$			8	
ΔV$_{os}$	Long-term input offset voltage drift [2]	V$_{icm}$ = 1 V		2.8		µV/√mo
		V$_{icm}$ = 12 V		1.0		
CMR	Common mode rejection	V$_{icm}$ = -20 to 70 V, DC mode	90	120		dB
		T$_{min}$ < T < T$_{max}$	85			
I$_{ib+}$	Input bias current	V$_{icm}$ = 12 V		350		µA
		T$_{min}$ < T < T$_{max}$, V$_{icm}$ = -20 to 70 V	-400		600	
I$_{ib-}$	Input bias current	V$_{icm}$ = 12 V		100		
		T$_{min}$ < T < T$_{max}$, V$_{icm}$= - 20 to 70 V	-100		350	
|V$_{sense}$|	Vsense operating range with Eg ≤ 0.3% [3]	TSC2011			78	mV
		T$_{min}$ < T < T$_{max}$			77.6	
Output						
G	Gain	TSC2011		60		V/V
Eg	Gain error vs. temperature	ΔV$_{out}$ = 100 mV to (V$_{cc}$ - 100 mV)			0.3	%
		T$_{min}$ < T < T$_{max}$			0.3	
ΔEg/ΔT	Gain error drift	T$_{min}$ < T < T$_{max}$			10	ppm/°C
NLE	Linearity error	V$_{icm}$ = 12 V		0.03		%
V$_{cc}$ - V$_{oh}$	Drop voltage output high	I$_{source}$ = 0.2 mA		15	30	mV
		T$_{min}$ < T < T$_{max}$			35	
V$_{ol}$	Output voltage low	I$_{sink}$ = 0.2 mA		26	40	
		T$_{min}$ < T < T$_{max}$			50	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{out}	Output current	Sink mode		36	60	mA
		$T_{min} < T < T_{max}$			50	
		Source mode	12	25		
		$T_{min} < T < T_{max}$	8			
Reg Load	Load regulation	I_{out} = - 10 to +4 mA		0.3	1.5	mV/mA
OFFSET adjustment						
R_t	Ratiometric accuracy			0.5		V/V
Acc	Accuracy, RTO	Voltage applied to Vref1 and Vref2 in parallel		0.1		%
Dynamic performance						
BW	Small signal -3 dB bandwidth	R_l = 10 kΩ, C_l = 100 pF	600	750		kHz
		$T_{min} < T < T_{max}$	300			
SR	Slew rate	R_l = 10 kΩ, C_l = 100 pF, V_{icm} = 1 V	6.2	8		V/µs
		$T_{min} < T < T_{max}$	4.8			
E_n	Noise, RTI	0.1 Hz to 10 Hz		37		µVpp
	Spectral density, RTI	f = 1 kHz		100		nV/√Hz
Shutdown function (active high)						
V_{il}	Logical low level		0		$0.3 x V_{cc}$	V
V_{ih}	Logical high level		$0.7 x V_{cc}$		V_{cc}	
I_{ih}	Leakage current	V_{shdn} = V_{cc} (Shutdown mode)		1.2		µA
T_{on}	Turn-on time	V_{shdn}= 2.7 V to 0 V, R_l = 10 kΩ		6		µs
T_{off}	Turn-off time	V_{shdn} = 0 V to 2.7 V, R_l= 10 kΩ		3		µs
I_{out}	Output leakage current	Shdn active		50		nA

1. RTI stands for "Related to input".

2. Typical value is based on the offset drift observed after 1000 h at 125 °C and extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV.

3. V_{sense} = (V_{in+}) − (V_{in-}).

4.1 Typical characteristics

Figure 3. Supply current vs. supply voltage

Figure 4. Supply current vs. input common mode

Figure 5. Supply current vs. temperature

Figure 6. Supply current vs. input common mode with active shutdown mode

Figure 7. **Input bias current vs. input common mode with shutdown active**

Figure 8. **Input bias current vs. temperature V$_{CC}$ = 2.7 V**

Figure 9. **Input bias current vs. temperature with V$_{CC}$ = 5 V**

Figure 10. **Input offset voltage vs. temperature**

Figure 11. Input offset voltage vs. input common mode with V_CC = 2.7 V

Figure 12. Input offset voltage vs. input common mode with V_CC = 5 V

Figure 13. Input offset voltage vs. supply voltage

Figure 14. Output current vs. output voltage

Figure 15. V_oh and V_ol vs. input common mode voltage with V_CC = 5 V

Figure 16. (Output voltage - V_ref) vs. V_sense unidirectionnal with V_CC = 5 V

Figure 17. (Output voltage - V_ref) vs. V_sense bidirectionnal with V_CC = 5 V

Figure 18. Output rail linearity vs. load with V_CC = 5 V

Figure 19. Linearity vs. V$_{sense}$ with V$_{CC}$ = 5 V

Figure 20. Linearity vs. V$_{sense}$ and temperature

Figure 21. Gain error vs. input common mode

Figure 22. Gain error vs. input common mode and temperature

Figure 23. Load regulation with V_{CC} = 5 V

Figure 24. Gain vs. frequency

Figure 25. Gain vs. frequency for different loads

Figure 26. Bandwidth vs. input common mode

Figure 27. Overshoot vs. capacitive load

Figure 28. Small signal response with V_{CC} = 5 V

Figure 29. Small signal response with V_{CC} = 2.7 V

Figure 30. Large signal response with V_{CC} = 5 V
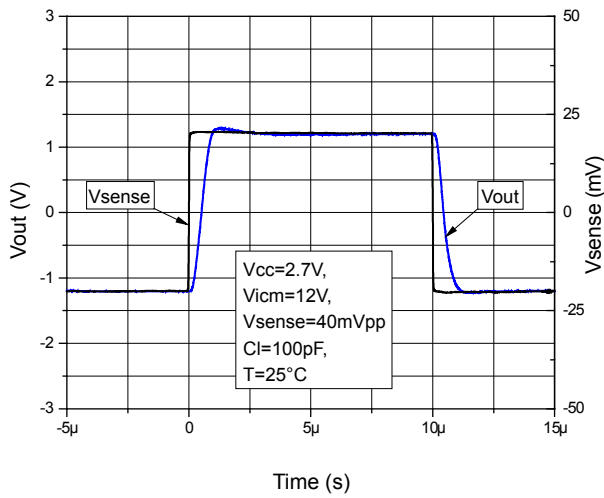
Figure 31. Large signal response with V$_{CC}$ = 2.7 V

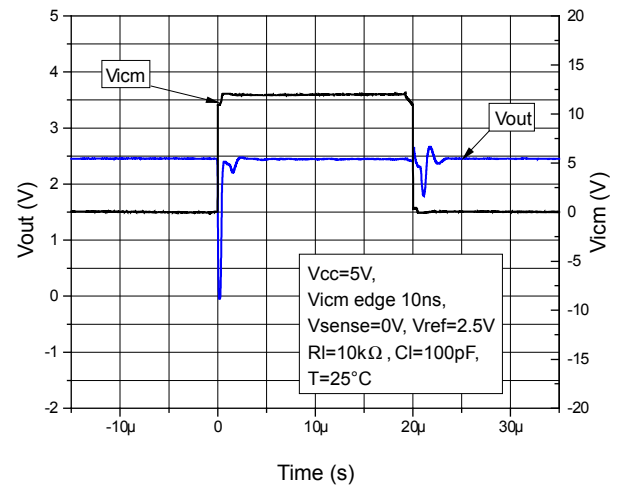**Figure 32. 12 V common mode step response recovery**

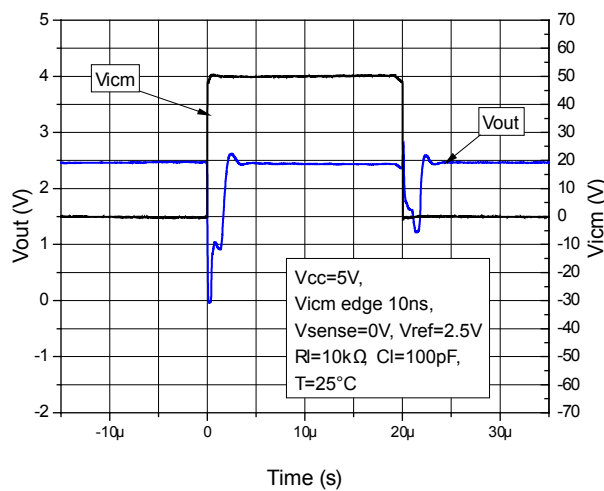**Figure 33. 50 V common mode step response recovery**

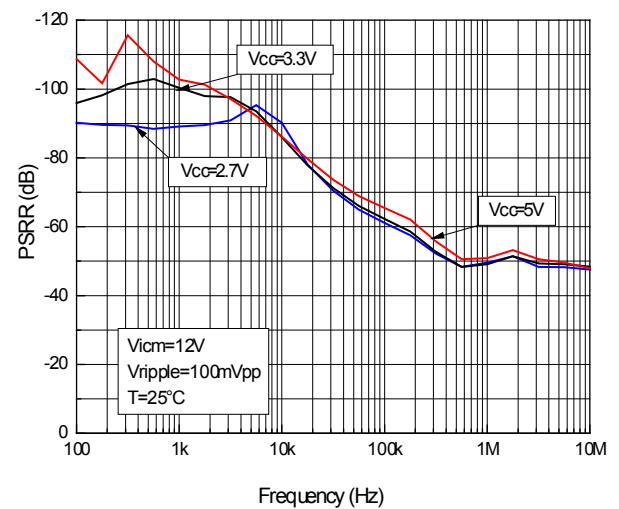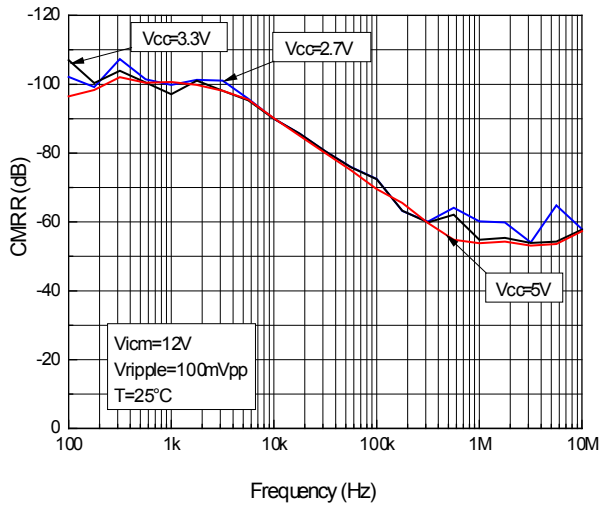**Figure 34. PSRR vs. frequency**

Figure 35. CMRR vs. frequency

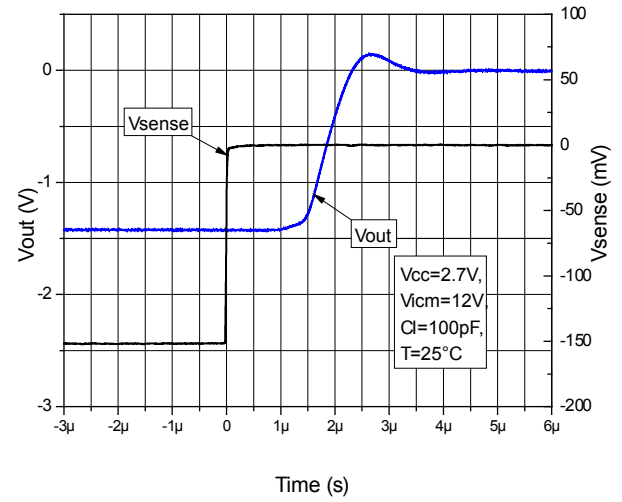**Figure 36. Positive overvoltage recovery V$_{CC}$ = 2.7 V**

Figure 37. Negative overvoltage recovery V$_{CC}$ = 2.7 V
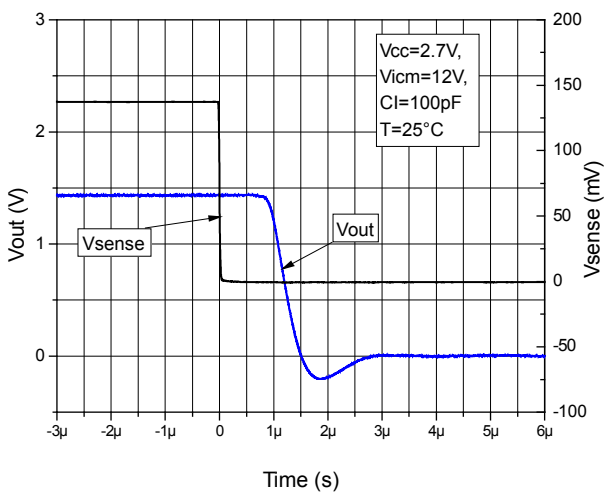

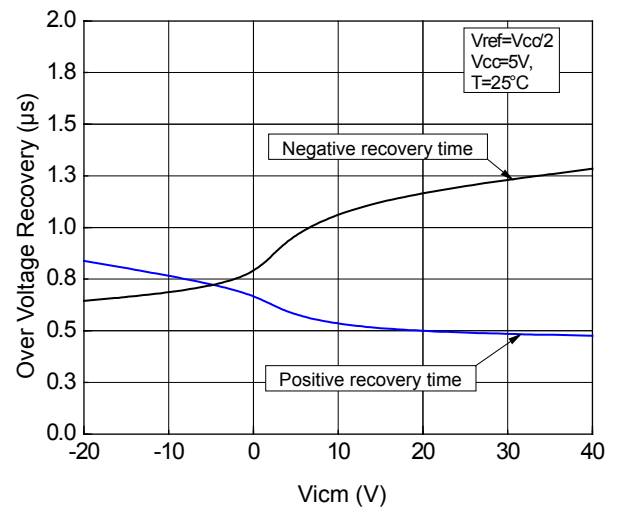**Figure 38. Overvoltage recovery vs. V$_{icm}$, V$_{CC}$ = 5 V**

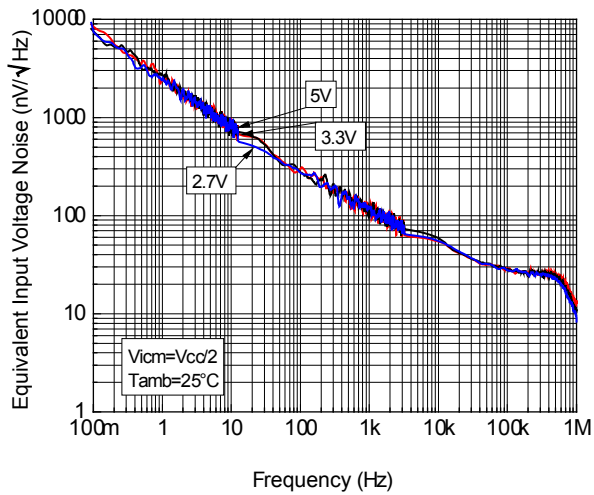**Figure 39. Noise vs. frequency**

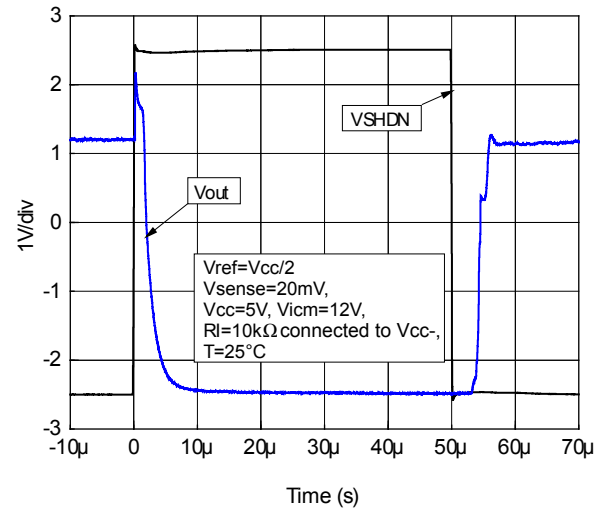**Figure 40. ON/OFF delay for shutdown mode**

Figure 41. Output voltage vs. V$_{sense}$ beyond the sense operating
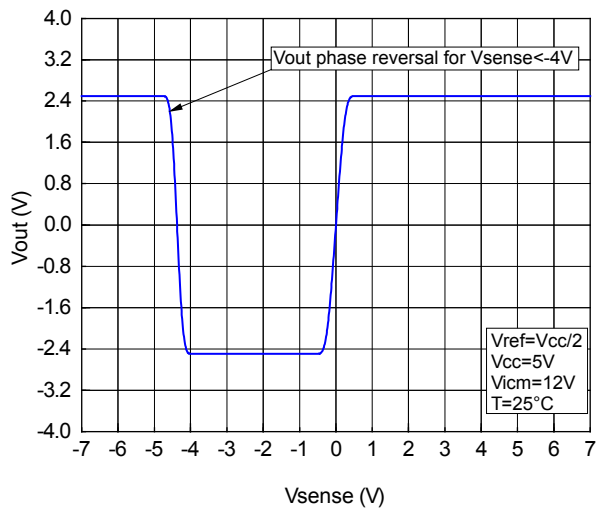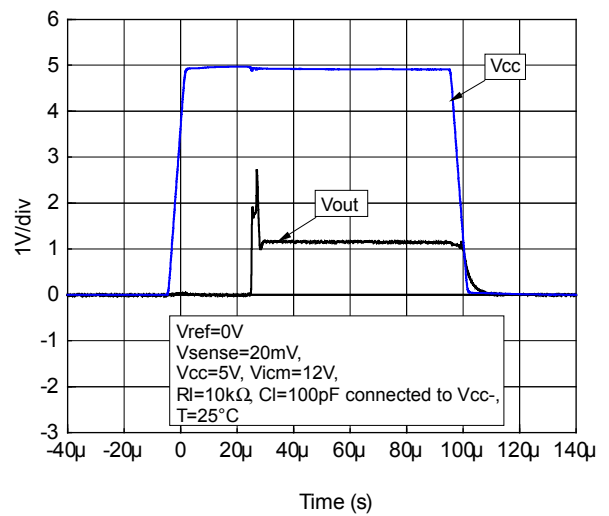

Figure 42. Power up time delay

5 Application information

5.1 Overview

The TSC2011 is especially designed to accurately measure the current by amplifying the voltage across a shunt resistor connected to its input. This voltage drop V_{sense} is then amplified by an instrumentation amplifier providing a max. input offset voltage of 500 µV (25°C) for an input common voltage of 12 V.

The TSC2011 is a fixed gain current sensing amplifier of 60 V/V. Thanks to a thin film resistor, the TSC2011 offers an extremely precise gain and a very high CMRR performance even in a high frequency range. Moreover, by fixing the output common mode voltage, the TSC2011 can be either used as unidirectional or bidirectional current sensing amplifier.

The TSC2011 provides an extended input common range from - 20 V below the negative supply voltage, and up to 70 V allowing either low-side or high-side current sensing, while the TSC2011 device can operate from 2.7 to 5.5 V.

The parameters are very stable in the full V_{cc} range and characterization curves show the TSC2011 characteristics at 2.7 V and 5.0 V. Moreover, the main specifications are guaranteed in an extended temperature range from -40 to 125 °C.
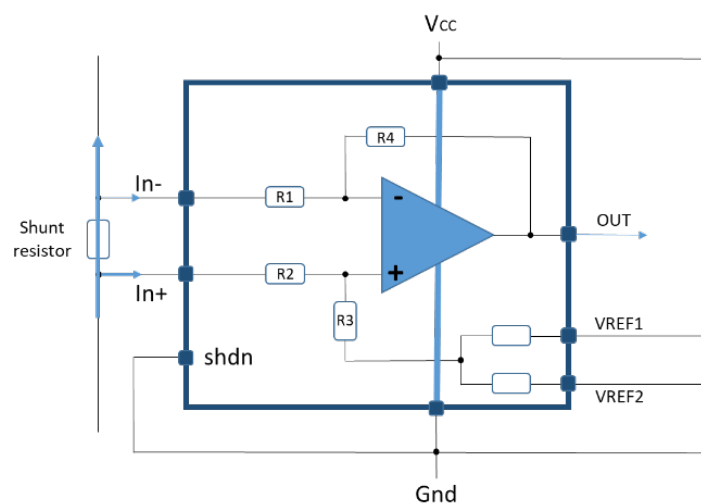
5.2 Theory of operation

The main feature of the TSC2011 is the ability to work with an input common mode voltage largely beyond the power supply V_{cc} range (2.7 V to 5.5 V). It is ideal, for example for automotive applications where a reverse battery can be supported by the TSC2011 without any damage. It also works with 48 V battery applications as the TSC2011 can support and measure the current on line at voltage up to 70 V. No additional protective components are needed in that range.
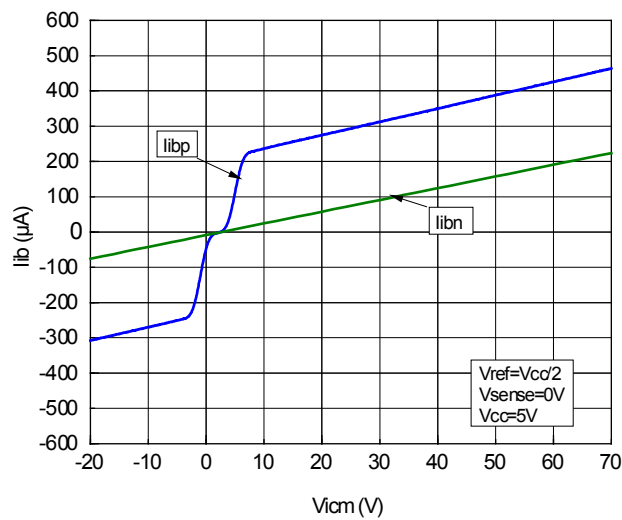
- $V_{cc} < V_{icm} < 70\ V$

In this case, the power supply of the TSC2011 is issued by the input and not only by the V_{cc} power supply. More precisely, a current is drawn by the common mode rail as depicted in the Figure 43. Power supply when $V_{icm} > V_{cc}$ to power it.

Figure 43. Power supply when $V_{icm} > V_{cc}$

In Figure 44. Input bias current vs. common mode voltage V_{cc} = 5 V, the current used to power the TSC2011 increases together with the V_{icm} voltage. The slope represents the internal common mode resistances. The most part of the current is drawn by the pin In+ as we can see on the i_{ibp} curve of Figure 9. Input bias current vs. temperature with V_{CC} = 5 V the current is around 450 µA. Some of it being V_{icm} / (R_4+R_1) and some supplies the input stage of the circuit, roughly 250 µA. On the In- pin 250 µA is drawn only.

So due to the architecture of the TSC2011, the current to be measured must be much larger than the input bias current. In case of small current to measure the Iib current must be taken into account.

Figure 44. Input bias current vs. common mode voltage V_{cc} = 5 V
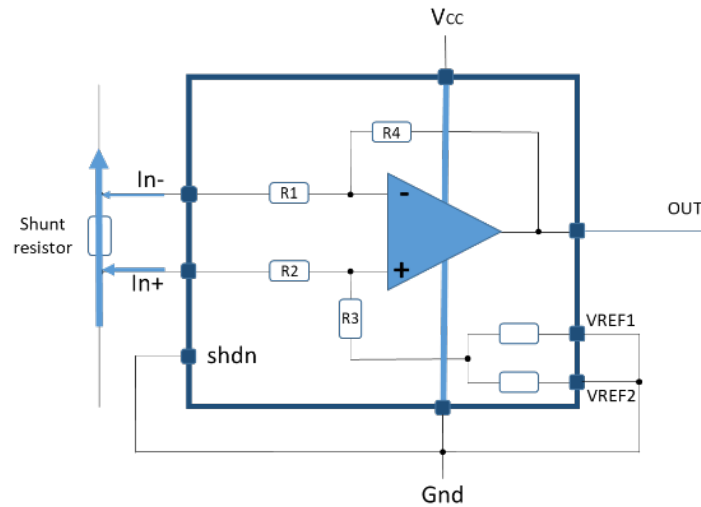

- **Gnd < V_{icm} < V_{cc}**

In this manner, the TSC2011 is only powered by the power supply V_{cc}, and the iib currents are very close to 0 µA and do not have any impact on the current measurement.

- **- 20 V < V_{icm} < Gnd**

The TSC2011 is fully functional in this range of common mode voltage and has also been characterized.

As the high positive common mode voltage, in this specific range, the TSC2011 is also powered by the input, see Figure 45. Power supply when V_{icm} < Gnd.

Figure 45. Power supply when V$_{icm}$ < Gnd

Most part of the current is still due to the pin I$_{n+}$ as we can see on the i$_{ibp}$ curve of Figure 9. Input bias current vs. temperature with V$_{CC}$ = 5 V. The current is about - 300 µA, some of it being V$_{icm}$ / (R$_4$ + R$_1$) and some other supplies the circuit, roughly 250 µA. A small part of the current, coming from the common mode rail, is also due to the input I$_{n-}$ in order to power the TSC2011, in a range of - 100 µV.
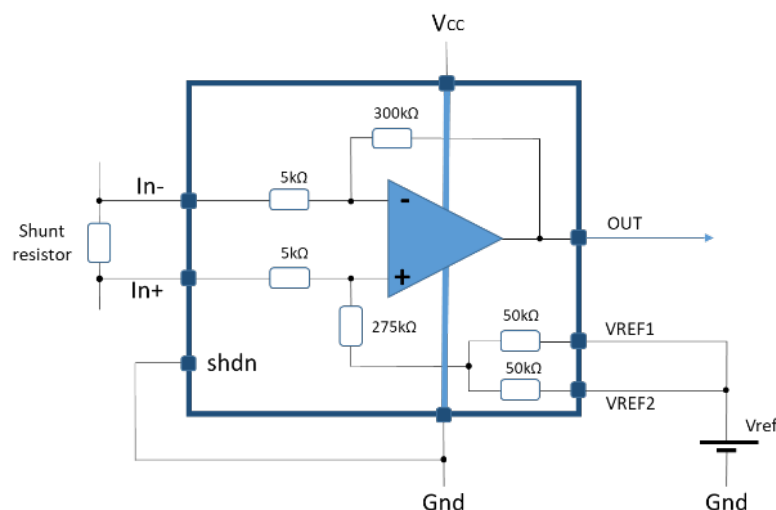
- **Output common mode range**

The TSC2011 output common mode voltage level can be set thanks to voltages applied on the Vref1 and Vref2 pins. These two pins allow the device to be set either in bidirectional or in unidirectional operation. The voltage applied to those pins must not exceed the V$_{CC}$ range. The different configurations are detailed in the section Unidirectionnal/Bidirectionnal operation.

As depicted by the Figure 46. V$_{ref}$ powered by an external voltage source, Vref1 and Vref2 pins can be driven by an external voltage source capable of sourcing/sinking a current following the equation below:

$$Iref = \frac{Vicm - Vref}{5k\Omega + 275k\Omega + 25k\Omega}$$

(1)

Figure 46. V$_{ref}$ powered by an external voltage source

When the output common mode voltage is supplied by an external power supply, in order to improve the output voltage measurement, it is recommended to measure the V_{out} differentially with respect to V_{ref} voltage. It provides a better CMRR measurement, better noise immunity and also a more accurate V_{out} voltage. A decoupling capacitance of 1 nF minimum can be also added to better filter the power supply, and can also be used as a tank capacitance in case an ADC is connected to this reference voltage.
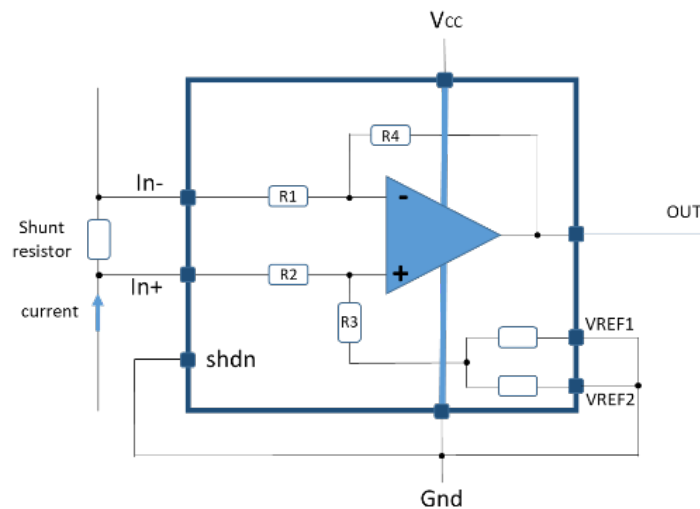
5.3 Unidirectionnal / bidirectionnal operation

- **Unidirectional operation**

Unidirectional mode of operation allows the device to measure the current through a shunt resistor in one direction only. The output reference can be ground or V_{cc} and can be set by using Vref1 and Vref2 pins for adjustment.
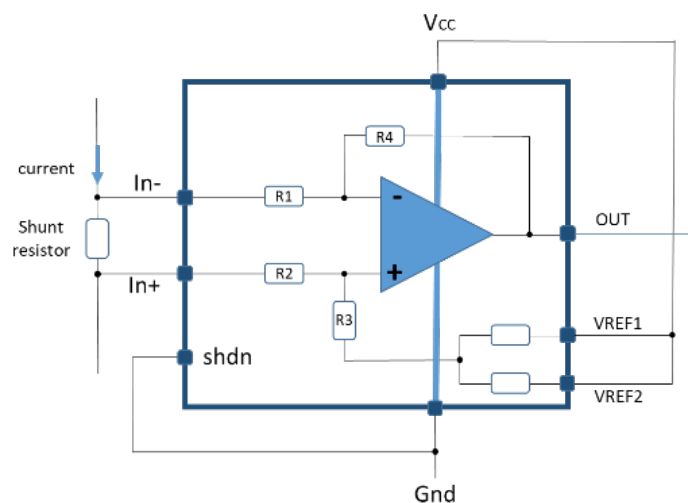
- **Ground referenced**

Figure 47. Output reference to ground

In this configuration Vref1 pin and Vref2 pin are connected together to the ground. The output common mode voltage is then automatically set to GND when no current flows through the R_{shunt} resistance. This configuration allows the full scale output in unidirectional mode. It allows a current to be measured as described in Figure 47. Output reference to ground.

- **V_{cc} referenced**

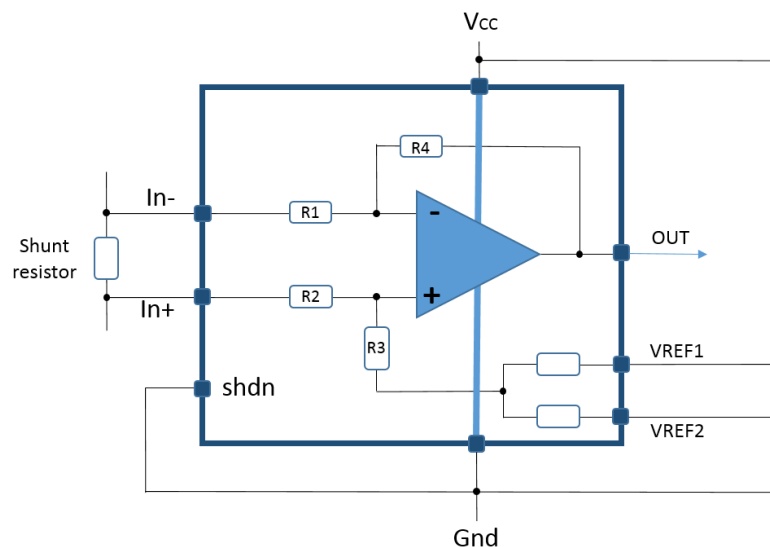**Figure 48. Output reference to V_{cc}**

In this configuration Vref1 pin and Vref2 pin are connected together to the V_{cc} power supply. The output common mode voltage is then automatically set to V_{cc} voltage when no current flows through the R_{shunt} resistance. This configuration allows the full scale output in unidirectional mode. It measures the current as described in Figure 48. Output reference to V_{cc}.

- **Bidirectional operation**

Bidirectional mode of operation allows the device to measure currents through a shunt resistor in two directions. The output reference can be set anywhere within the power supply range. If the output common mode voltage is set at mid-range, the full scale current measurement range is equal in both directions. This is achieved by connecting one Vref pin to Vcc and the other Vref pin to Gnd as described by Figure 49. Split supply. It can be done as well connecting both Vref pins to V_{cc} / 2 voltage as described by Figure 50. External supply. In case the current measurement is not equal in both directions, user can set the output in a non-symmetrical configuration, adjusting Vref according to the user's needs.
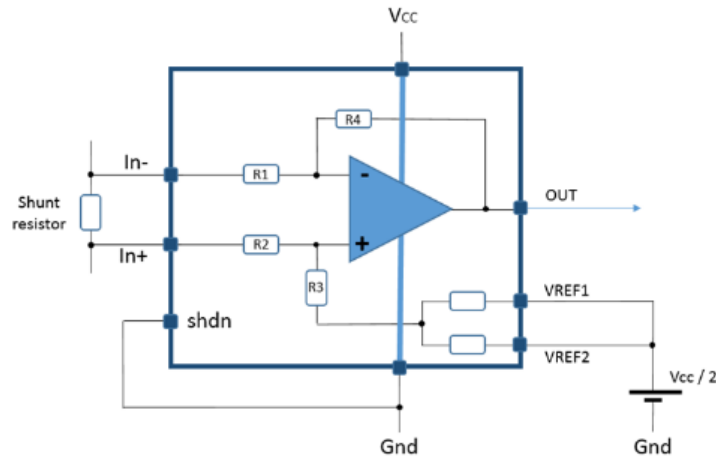
- **Split supply**

Figure 49. Split supply

The great advantage of this configuration, is that the TSC2011 can be used in bidirectional mode with an output common mode voltage set at the middle of scale, with an accuracy of 0.1%, without any added external component or power supply. This configuration creates a midscale offset ratiometric to the power supply.

- **External**

Figure 50. External supply

In this configuration, Vref1 pin and Vref2 pin are connected together to a reference voltage. The output common mode voltage is then automatically set to this reference voltage value when no current flows through the R_{shunt} resistance. This configuration adjusts the output offset as needed by the application. A DAC for calibration of the analog chain could also be used.

5.4 R_{SENSE} selection

The selection of the shunt resistor is a tradeoff between the dynamic range and power dissipation.

Generally, in high current sensing application, the main focus is to reduce as much as possible the power dissipation (I²R) by choosing the smallest value of shunt. It could be quite easy if a full scale current to measure is small.

In low current applications the R_{sense} value could be higher, to minimize the impact of the offset voltage on the circuit. Due to input bias current of several µA, the TSC2011 cannot measure the current in the same range, when the common mode voltage overpasses the power supply voltage (refer to section about theory of operation).

The tradeoff is mainly when a dynamic range of current to measure is large, meaning ability to measure with the same shunt value from low current to high current. Generally, the current full scale (Imax-Imin) defines the shunt value thanks to the full output voltage range, the gain of the TSC2011. The TSC2011 can work with a full scale ΔV_{out} = 100 mV to V_{cc} - 100 mV with maximum gain accuracy of 0.3%.

At first order, the full current range to measure through R_{sense} can be defined by equation 2, just by taking the gain error and input offset voltage as inaccuracy parameters:

$$Isense\_full\_scale*Rsense = \frac{Vcc - 200mV}{TSC\_Gain(1 + Eg)} - 2\left|Vio\right| \qquad (2)$$

The V_{sense} parameter is defined in the electrical characteristics following the equation 2.

Its purpose is to highlight that the product $R_{sense}*T_{SC\_gain}$ is determined by the application, and that once one of these two parameters is selected, the maximum value of the second one can be calculated.

- If power dissipation in the shunt is the key point, R_{Sense} should be chosen as follows:

$$Rsense \leq \frac{Pmax}{Imax^2}$$

and then choosing the right gain. For example, for high current to sense, the TSC2012 can offer a gain of 100, in this manner a smaller shunt can be used and so limited power losses. However accuracy can be lower.

- Or choosing the product available on the shelf, and then size the shunt resistor value accordingly.

5.5 Input offset voltage drift overtemperature

The maximum input offset voltage drift overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using equation 3:

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) \ - V_{io}(25°C)}{T - \ 25°C}\right| \tag{3}$$

Where T = -40 °C and 125 °C.

The TSC2011 datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.6 Error calculation

The principal source of error, such as: input offset voltage, gain error, common mode rejection ration, are described separately in the electrical characteristics. This chapter summarizes the most important error to take into account during a design phase.

- **Input offset voltage error**

The equation 2 depicts a first order error calculation just by taking into account the input offset voltage. In a temperature environment, the deviation of the V_{io} and the error linked to the input offset on the output voltage can be written as equation 4:

$$Vio\ Error = (\pm Vio \pm Dvio/Dt)*Gain \qquad (4)$$

- **Gain error and shunt resistance accuracy**

$$Gain\ error = Gain(1 + \varepsilon gain) \qquad (5)$$

$$Rsense\ error = Gain(1 + \varepsilon Rsense) \qquad (6)$$

Where $\varepsilon gain$ is the gain error 0.3% max for the TSC2011.

Where $\varepsilon Rsense$ is the shunt resistance error. Shunt resistors from 5 mΩ to 100 mΩ are available with 1% accuracy or better.

- **CMR error**

In the electrical characteristics, CMR is specified at one input common mode voltage. So in order to take into consideration the variation of the input voltage offset depending the V_{icm}, the calculus must be done till this known point. Let us get the V_{icm} = 12 V as reference point.
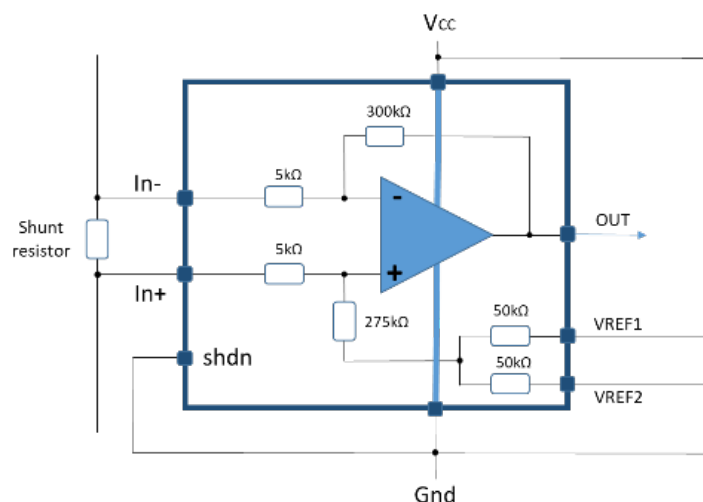
So the error on V_{out} due to a common mode voltage variation can be written as the equation 7:

$$CMR\ error = \pm \frac{Vicm - 12V}{CMR}*Gain \qquad (7)$$

- **Output common mode error (Vocm)**

This error can be taken into account when the output common mode voltage is set like suggested in the Figure 51. Schematic for V_{ocm} error, and so by using the internal divider bridge. Otherwise it is important to take into consideration the error linked to the voltage source applied on the V_{Ref1} pin and V_{ref2} pin.

Figure 51. Schematic for V_{ocm} error

The divider bridge is made by two resistances of 50 kΩ given an output common mode voltage of:

$$\frac{Vref1 + Vref2}{2}$$

Due to a small mismatch of the internal resistance the error, on the output common mode voltage, can be described as equation 8:

$$Vocm = \left(\frac{Vref1 + Vref2}{2}\right).(1 + \varepsilon Acc) \tag{8}$$

Where εAcc is the accuracy referred to the output with a typical value of 0.1%.

- **Noise**

The Figure 39. Noise vs. frequency expresses the noise referred to the input of the TSC2011. This device shows a 1/f noise until 10 kHz frequency. Above this limit the white noise density is 29 nV/$\sqrt{Hz}$, until the bandwidth of the TSC2011.

The noise can be then expressed as two terms, the former related to the 1/f noise and the latter due to the white noise. If we consider that there is no additional filter on the TSC2011 and it is only bandwidth limited, it can be considered that over the 750 kHz, there is an attenuation of the noise with a first order filtering. So the equivalent noise bandwidth is $750 kHz.\frac{\pi}{2}$.

The RMS value of the output noise is the integration of the spectral noise over the bandwidth of interest and can be expressed as equation 9:

$$enRMS = \left(\sqrt{\int_{0.1}^{10000}\left(\frac{29.10^{-9}}{\sqrt{\frac{f}{10.10^3}}}\right)^2 df + \int_{0.1}^{750000.\frac{\pi}{2}}\left(29.10^{-9}\right)^2 df}\right)*Gain \tag{9}$$

- **Total error**

The maximum total error expected on the output of the device can be described as the sum of the different source described just above. The total output accuracy can be written as equation 10.

$$Vout_{err} = Gain*Rsense*|Iload|(\varepsilon gain + \varepsilon Rsense) + Gain.|Vio| + Gain.\frac{|Vicm - 12V|}{CMR} + \tag{10}$$

$$|Vocm|(\varepsilon Acc) + noise$$

I$_{load}$ is described in Figure 52. Input current and the output noise is described by the equation 9.

Note that the input bias currents are not taken into account in this section, as they are already integrated in the V$_{sense}$. The Figure 52. Input current below depicts the current flowing from the source to the load when the input common mode voltage is higher than the supply voltage.

Figure 52. Input current

From a calculation approach, when V$_{icm}$ voltage is beyond V$_{cc}$, I$_{load}$ must be considered as the sum of I$_{source}$ and Input bias current (I$_{ib}$). Note that the input bias current on the pin – is largely lower and can be neglected.

The Figure 52. Input current also expresses that the TSC2011 cannot measure the current in the same order as input bias current (several hundreds of µA).

The linearity is not taken into account in the error calculus as it represents 0.03% of error only and it is negligible. Nevertheless, as the gain error has been calculated thanks to the best fit line approach, it gives the information that the gain error can be relatively constant throughout the linear input range of the TSC2011.

The equation 10 has been described for a temperature of 25 °C. For sure with a temperature variation, D_{vio}/DT error term must be added. And if the power supply is susceptible to change, the SVR parameter must also be taken into account.

- **Example**

Let us consider that the maximum total error can happen on the output of the TSC2011.

- **Use case:**
  - V_{cc} = 5 V
  - V_{icm} = 24 V
  - V_{ocm} = 2.5 V
  - Temperature = 25 °C
  - I_{load} = 5 A
  - Shunt 5 mΩ with 1% accuracy

Theoretically the expected output voltage should be V_{out} = R_{shunt} * I_{load} *60 + V_{ocm} = 4 V.

From the equations above, all the error terms are detailed by using the maximum value of the electrical characteristics (when available), in order to express as much as possible, the worst case condition. The % error on output of the following table is expressed in reference of $V_{out} - V_{ref}$, so in this typical example: 1.5 V.

Table 6. Gain error

Error source	Calculus	Output voltage error	% error on output
Gain error	$60*5 . 10^{-3}*5*0.3\%$	4.5 mV	0.3%
V_{io} error	$60*500\mu V$	30 mV	2%
CMRR error	$60*\dfrac{24V - 12V}{10^{\frac{90}{20}}}$	22.7 mV	1.5%
V_{ocm} error	$2.5*0.1\%$	2.5 mV	0.2%
Noise	$60*\dfrac{29nV}{\sqrt{Hz}}\sqrt{10kHz*\left(\ln(10k) - \ln(0.1)\right) + 750kHz*\dfrac{\pi}{2} - 0.1Hz}$	1.98 mV$_{RMS}$	0.4% [1]
Total		60 mV +1.98 mV$_{RMS}$	4.4%

1. *The percentage is based on voltage peak value, which is 3 times RMS value.*

So the maximum output voltage in the worst case condition at ambient temperature is 4.060 V + 1.98 mV$_{RMS}$ instead of 4 V expected. This represents an error on the current reading about 4.4%. 1% more must be added due to the shunt accuracy.

This calculus comes from all the maximum values and all the error terms which have been added to each other, meaning that the chance to get 4.4% precision in the use case above is extremely low and on the whole population, the error is largely smaller.
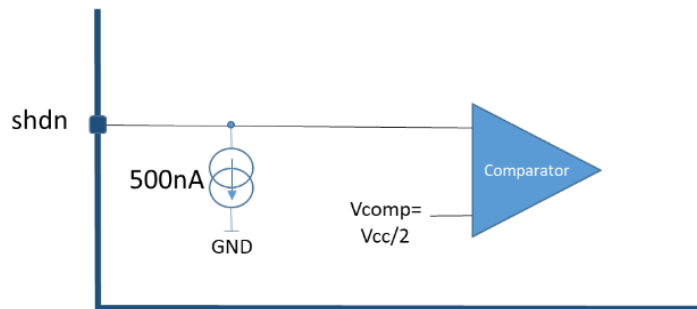
5.7 Shutdown mode

If the SHDN pin is driven between 0.7 x V_{cc} and V_{cc} the TSC2011 enters low power shutdown mode, drawing less than 20 µA, over the V_{cc} and V_{icm} range. In SHDN mode the output is in HiZ state.

Although there is an internal current source of 500 nA on the SHDN pin, keeping a low state allowing the TSC2011 to work without any voltage applied on the SHDN pin, it is strongly recommended to apply the dedicated voltage on the SHDN pin to ensure the full functionality of the TSC2011, especially when fast common mode variation appears.

The figure below depicts the architecture of the SHDN pin.

Figure 53. **SHDN pin**

- With GND applied to SHDN pin the TSC2011 is in active mode
- With V_{cc} applied to SHDN pin the TSC2011 is in shutdown mode

5.8 Stability

- **Driving switched capacitive loads**

Some ADCs get their signal thanks to a sample and hold capacitor. If before a sampling this capacitance is fully discharged, a fast current load can appear on the output of the TSC2011 during the sampling phase.

The scope probe in the figure below shows the output voltage of the TSC2011 excited by a 40 pF capacitor with a 3.3 Vpp signal at 50 kHz to simulate the sample and hold circuit of the ADC120.

Figure 54. **Capacitive load response at V_{cc} = 3.3 V**

The ADC120 has a conversion rate of 50 ksps, which is perfect to sample and hold the output of the TSC2011 without any error.

The graph shows the behavior of the output of the TSC2011 under the worst case condition, as for example, when there is an ADC120 channel change between two measurements.

If a single channel is used, for sure the change on the sample and hold capacitance are very small, and so the recovery time is extremely low as described by the figure below.

Figure 55. Capacitive load response at V_{cc} = 3.3 V with a step of 100 mV

The effect of the ADC sampling and hold can be easily smoothed thanks to an RC filter. As suggested on the schematic below. The capacitor of the external filter must be chosen much higher than the internal ADC capacitor, in order to easily absorb the sudden voltage variation on the output due to the sampling and hold of the ADC. The resistance must be chosen accordingly to the application speed of the system in order not to impact the whole application. The main advantage of using an RC filter is to have an antialiasing system. For sure the used ADC must have sample and hold conversion in accordance with the RC filter value, in order to let the output recover before sampling.

Figure 56. RC filter when driving ADC

In the figure Figure 57. Capacitive load response at V_{cc} = 3.3 V with 720 kHz RC filter an R_s = 470 Ω resistance and a C_t = 470 pF capacitance have been set. Given a low-pass filter of 720 kHz and a response time of roughly 660 ns.

In the figure Figure 58. Capacitive load response at V_{cc} = 3.3 V with 194 kHz RC filter an R_s = 820 Ω resistance and a C_t = 1 nF capacitance have been set. Given a low-pass filter of 194 kHz and a response time of roughly 2.5 μs.

Figure 57. Capacitive load response at V$_{cc}$ = 3.3 V with 720 kHz RC filter

Figure 58. Capacitive load response at V$_{cc}$ = 3.3 V with 194 kHz RC filter

The value of the added external capacitor must be taken into account. Indeed, if this one is chosen with an excessive value and the serial resistance with a too small value, the risk of instability on the output of the TSC2011 is high.

- **Driving large capacitive C$_{load}$**

Increasing the load capacitance produces gain peaking in the frequency response, with an overshoot and ringing in the step response.

The figure below, shows the serial resistors that must be added to the output, to make a system stable. The chosen criteria ensures the stability of the system and it is an overshoot lower than 24%.

Figure 59. Stability criteria with a serial resistor at V$_{CC}$ = 5 V

5.9 Power supply recommendation

In order to decouple correctly the TSC2011, a 100 nF bypass capacitor can be placed between V_{cc} and Gnd. This capacitor must be placed as closer as possible to the supply pins. The figure below shows a start-up time with a decoupling capacitance of 100 nF.

Figure 60. Start-up time with a decoupling capacitance of 100 nF

V_{ref} pin is used to fix the output common mode voltage and it is driven by a low impedance voltage source and can be decoupled thanks to a 10 nF bypass capacitor.

A greater bypass capacitor added on V_{cc} pin and V_{ref} pin helps to enhance CMRR and PSRR performance.

5.10 PCB layout recommendations

The layout of the PCB tracks connected to the current sensing, load and power supply is very important. It is a good practice to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

When a shunt resistance, lower than 1 Ω, is used, a 4-wire connection technique should be used to sense the current as described in the schematic below. This technique separates pairs of current carrying and voltage-sensing electrodes to make more accurate measurements by eliminating the lead and contact resistance from the measurement.

The track connected to the input pin of the TSC2011 has to be considered as a differential pair, it must have the same length and width, and ideally placed on the same PCB plane, and above all must be routed as far as possible from noisy source. As this track carries the input bias current, in a range of hundreds of µA, it can be designed small but always by taking care of its resistivity. Any via in these input tracks are non-recommended to avoid any parasitic resistance in this path.

To minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

A ground plane generally helps to reduce EMI, that is why a multilayer PCB use is suggested as well as the ground planes as a shield to protect the internal track. In this case, the digital from the analog ground must be separated and any ground loop must be avoided. Loop area or antenna must be reduced to minimize EMI impact.

The Figure 61. Recommended layout suggests a possible routing for the TSC2011, in order to minimum parasitic effect.

Figure 61. Recommended layout

5.11 EMI rejection ration (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of current sensing device. An adverse effect that is common to many current sensing is a change in the offset voltage as a result of RF signal rectification. A first order internal low pass filter is included on the input of the TSC2011 to minimize susceptibility to EMIRR. Figure below shows the EMIRR on pin IN+, the EMIRR on pin IN- of the TSC2011 measured from 400 MHz up to 2.4 GHz.

Figure 62. EMIRR on pin+

Figure 63. EMIRR on pin-

5.12 Overload recovery

Overload recovery is defined as the time required for the current sensing output to recover from a saturated state to a linear state.

The saturation state occurs when the output voltage gets very close to rails in the application. It results from an excessive input voltage.

When the output of the TSC2011 enters saturation state, less than 1 µs is needed to get back to a linear state as shown by Figure 64. Negative overvoltage recovery V_{CC} = ± 2.5 V and Figure 65. Positive overvoltage recovery V_{CC} = ± 2.5 V.

Figure 36. Positive overvoltage recovery V_{CC} = 2.7 V and Figure 37. Negative overvoltage recovery V_{CC} = 2.7 V show the overvoltage recovery for a V_{CC} = 2.7 V.

Figure 64. Negative overvoltage recovery V_{CC} = ± 2.5 V

Figure 65. Positive overvoltage recovery V_{CC} = ± 2.5 V

5.13 Application examples

5.13.1 Half-bridge motor control

The half-bridge topology is very popular in motor control, DC-DC converters, LED lighting control and other bidirectional loads from a single supply potential.

The TSC2011 provides a feedback control system about current but also detects overload conditions.

The Figure 66. Half-bridge application describes a typical schematic using the TSC2011 in a motor control application. A 20 mΩ shunt resistance in series with the motor monitors a measurable voltage drop representing the load current, and the TSC2011 amplifies the V_{sense} in order to give some information about the current flowing into the motor in real time. These information are then digitalizing by the 12-bit ADC (ADC120).

Figure 66. Half-bridge application

General overview:

To make the motor rotation occur, the NMOS H1, H2, L1, L2 are driven by a half-bridge quad power MOSFET driver. We have to consider that the current flows from the 12 V to the GND, through H1 NMOS and L2 NMOS. A PWM is applied on the NMOS L2 in order to control the current and thus the speed of the motor.

By PWM, the average voltage applied on the motor is controlled. H1 remains always ON and the PWM is applied on L2. When L2 is turned off, H2 must be turned ON, for freewheeling, allowing the discharge of the motor inductance current. This phenomenon generates a fast input common mode voltage transition on the TSC2011, from 0 V to 12 V.

Thanks to a good recovery time due to fast input common mode change, the TSC2011 follows the current flowing into the motor as depicted by the scope probe in Figure 67. TSC2011 H Bridge application.

The black curve represents the fast V_{icm} variation step of 12 V in 500 ns when the freewheeling is activated. The blue curve represents the current flowing into the motor measured with a current probe.

The red curve represents the output voltage - 1.35 V (Vref voltage) of the TSC2011 probe after the RC filter.

The RC filter, used to drive the ADC120, smooths a bit the output signal and adds a small constant time, in the range of 1 µs.

Figure 67. TSC2011 H Bridge application

After a fast variation of the input common mode, the TSC2011 needs less than 5 µs to recover its normal behavior.

5.13.2 Solenoid valve

In automotive applications, the automatic transmission relies on bands and clutches to change gears, and the only way they can be applied is by fluid pressure. The transmission solenoid is responsible for opening or closing valves in the valve body to allow transmission fluid to enter, at which point the fluid can pressurize the clutches and bands. Solenoids consist of a spring loaded plunger wrapped with a coil of wire, and it is generally driven thanks to a MOS transistor.

In the schematic below the TSC2011 is used in mono directional mode. When the MOS is ON, the current can flow through the solenoid and actuate this one. The input common mode is high in this case.

When the MOS is turned OFF, as the current stored into the solenoid cannot stop instantaneously, the diode turns ON allowing a freewheeling to discharge the solenoid resulting in a common mode one diode voltage drop below ground.

Thanks to its large input common mode range, the TSC2011 can be used for such applications depicted in figure below.

In order not to saturate the output when no current is flowing into R_{sense}, a small voltage on V_{ref} has to be applied.

Figure 68. **Solenoid valve application**

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SO8 package information

Figure 69. SO8 package outline

Table 7. SO-8 mechanical data

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

6.2 MiniSO8 package information

Figure 70. MiniSO8 package outline

Table 8. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

7   Ordering information

Table 9. Order codes

Order code	Gain (V/V)	Package	Packaging	Marking
TSC2011IDT	60	SO8	Tape and reel	TSC2011
TSC2011IST		MiniSO8		O118

Revision history

Table 10. Document revision history

Date	Revision	Changes
11-Sep-2019	1	Initial release.

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