CC2564MODN *Bluetooth*® Host Controller Interface (HCI) Module

1 Device Summary

1.1 Features

- Single-Chip Solution Integrating *Bluetooth* Basic Rate (BR)/Enhanced Data Rate (EDR)/Low Energy (LE) Features
- *Bluetooth* 4.1 Compliant Up to the HCI Layer
- BR/EDR Features Include:
  - Up to 7 Active Devices
  - Scatternet: Up to 3 Piconets Simultaneously, 1 as Master and 2 as Slaves
  - Up to 2 SCO Links on the Same Piconet
  - Support for All Voice Air-Coding – Continuously Variable Slope Delta (CVSD), A-Law, µ-Law, and Transparent (Uncoded)
- Assisted Mode for HFP 1.6 Wideband Speech (WBS) Profile or A2DP Profile to Reduce Host Processing and Power
- LE Features Include:
  - Support of Up to 10 Simultaneous Connections
  - Multiple Sniff Instances Tightly Coupled to Achieve Minimum Power Consumption
  - Independent Buffering for LE Allows Large Numbers of Multiple Connections without Affecting BR/EDR Performance.
  - Built-In Coexistence and Prioritization Handling for BR/EDR and LE
- Flexibility for Easy Stack Integration and Validation Into Various Microcontrollers, Such as MSP430™ and ARM® Cortex®-M3 and Cortex®-M4 MCUs
- Highly Optimized for Design into Small Form Factor Systems:
  - Single-Ended 50-Ω RF Interface
  - Module Footprint: 33 Terminals, 0.9-mm Pitch, 7 mm x 7 mm x 1.4 mm
- Best-in-Class *Bluetooth* (RF) Performance (TX Power, RX Sensitivity, Blocking)
  - Class 1.5 TX Power Up to +10 dBm
  - Internal Temperature Detection and Compensation to Ensure Minimal Variation in RF Performance Over Temperature, No External Calibration Required
  - Improved Adaptive Frequency Hopping (AFH) Algorithm with Minimum Adaptation Time
  - Provides Longer Range, Including 2x Range Over Other BLE-Only Solutions
- Advanced Power Management for Extended Battery Life and Ease of Design:
  - On-Chip Power Management, Including Direct Connection to Battery
  - Low Power Consumption for Active, Standby, and Scan *Bluetooth* Modes
  - Shutdown and Sleep Modes to Minimize Power Consumption
- Physical Interfaces:
  - Standard HCI Over H4 UART with Maximum Rate of 4 Mbps
  - Standard HCI Over H5 UART with Maximum Rate of 4 Mbps
  - Fully Programmable Digital PCM-I2S Codec Interface
- CC256x *Bluetooth* Hardware Evaluation Tool: PC-Based Application to Evaluate RF Performance of the Device and Configure Service Pack
- Lead-Free Design Compliant with RoHS Requirements
- Built-In CC2564B Single-Chip *Bluetooth* Device Fully Compliant with *Bluetooth*+EDR
- Supports Class 1.5 (High-Output Power) Applications
- Small Size with Low Power Consumption
- Supports Maximum *Bluetooth* Data Rates Over HCI UART Interface
- Supports Multiple *Bluetooth* Profiles with Enhanced QoS (Mono and Stereo) Assisted A2DP (No Host Processing Required)

1.2 Applications

- Mobile Accessories
- Sports and Fitness Applications
- Wireless Audio Solutions
- Remote Controls
- Toys

PRODUCT PREVIEW

1.3 Description

The CC2564MODN TI *Bluetooth* HCI module is a complete *Bluetooth* BR/EDR/LE HCI solution that reduces design effort and enables fast time to market. Based on TI's seventh-generation *Bluetooth* core, the HCI module provides a product-proven solution that is *Bluetooth* 4.1 compliant. When coupled with a microcontroller unit (MCU), the HCI module provides best-in-class RF performance.

TI's power-management hardware and software algorithms provide significant power savings in all commonly used *Bluetooth* BR/EDR/LE modes of operation.

With transmit power and receive sensitivity, this solution provides a best-in-class range of about 2x, compared to other BLE-only solutions. A royalty-free software *Bluetooth* stack available from TI is pre-integrated with TI's MSP430 and ARM Cortex-M3 and Cortex-M4 MCUs. The stack is also available for made for iPod® (MFi) solutions and on other MCUs through TI's partner Stonestreet One (www.stonestreetone.com). Some of the profiles supported today include: serial port profile (SPP), advanced audio distribution profile (A2DP), human interface device (HID), and several BLE profiles (these profiles vary based on the supported MCU).

In addition to software, this solution consists of a reference design with a low BOM cost. For more information on TI's wireless platform solutions for *Bluetooth*, see TI's Wireless Connectivity Wiki (processors.wiki.ti.com/index.php/CC256x).

Table 1-1. Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
XCC2564MODNCMOET	MOE (33)	7.1 mm x 7.1 mm
XCC2564MODNCMOER	MOE (33)	7.1 mm x 7.1 mm

1.4 Functional Block Diagram

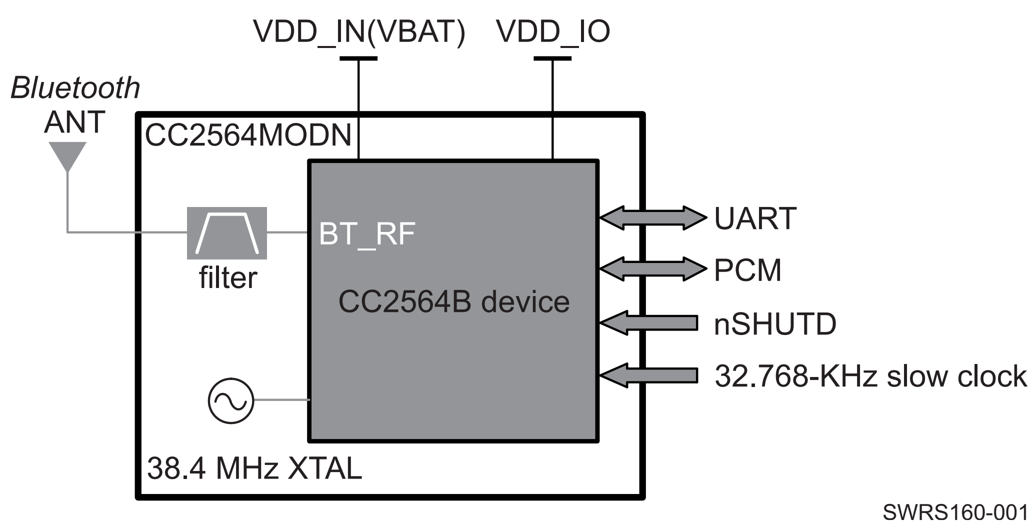


Figure 1-1. Functional Block Diagram

PRODUCT PREVIEW

Table of Contents

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2014) to Revision A	Page
• Deleted "Fully Compliant with the Bluetooth 4.0 Specification Up to the HCI Layer" in *Features*	1
• Added bullet in *Features*: "*Bluetooth* 4.1 Compliant Up to the HCI Layer"	1
• Changed "supports *Bluetooth* 4.0 dual-mode (BR/EDR/LE) protocols" to "*Bluetooth* 4.1 compliant" in *Description*	2
• Changed *Bluetooth* 4.0 + BLE to *Bluetooth* 4.1 + BLE and *Bluetooth* 4.0 + ANT to *Bluetooth* 4.1 + ANT in Table 3-1	4
• Changed "fully complies with the *Bluetooth* 4.0 specification" to "is *Bluetooth* 4.1 compliant in Section 3.1, *Bluetooth BR/EDR Features*	4
• Added Supports all roles defined by the *Bluetooth* v4.0 specifications in Section 3.2, *Bluetooth* LE Features	4

PRODUCT PREVIEW

3 Device Overview

Table 3-1. Technology and Assisted Modes Supported

Module	Description	Technology Supported			Assisted Modes Supported	
		BR/EDR	LE	ANT	HFP 1.6 (WBS)	A2DP
CC2564MODN	*Bluetooth* 4.1 + BLE	√	√		√	√
	Bluetooth 4.1 + ANT	√		√	√	√

3.1 *Bluetooth* BR/EDR Features

The TI *Bluetooth* HCI module is *Bluetooth* 4.1 compliant up to the HCI level (for the technology supported, see Table 3-1):

- Up to seven active devices
- Scatternet: Up to 3 piconets simultaneously, 1 as master and 2 as slaves
- Up to two synchronous connection oriented (SCO) links on the same piconet
- Very fast AFH algorithm for asynchronous connection-oriented link (ACL) and extended SCO (eSCO) link
- Supports typically 10-dBm TX power without an external power amplifier (PA), thus improving *Bluetooth* link robustness
- Digital radio processor (DRP™) single-ended 50-Ω I/O for easy RF interfacing
- Internal temperature detection and compensation to ensure minimal variation in RF performance over temperature
- Flexible pulse-code modulation (PCM) and inter-IC sound (I2S) digital codec interface:
  – Full flexibility of data format (linear, A-Law, µ-Law)
  – Data width
  – Data order
  – Sampling
  – Slot positioning
  – Master and slave modes
  – High clock rates up to 15 MHz for slave mode (or 4.096 MHz for master mode)
- Support for all voice air-coding
  – CVSD
  – A-Law
  – µ-Law
  – Transparent (uncoded)

3.2 *Bluetooth* LE Features

- *Bluetooth* 4.1 compliant
- Solution optimized for proximity and sports use cases
- Supports up to 10 (CC2564 or CC2564B) simultaneous connections
- Multiple sniff instances that are tightly coupled to achieve minimum power consumption
- Independent buffering for LE, allowing large numbers of multiple connections without affecting BR/EDR performance.
- Includes built-in coexistence and prioritization handling for BR/EDR and LE

NOTE

ANT and the assisted modes (HFP 1.6 and A2DP) are not available when BLE is enabled.

3.3 *Bluetooth* Transport Layers

Figure 3-1 shows the *Bluetooth* transport layers.

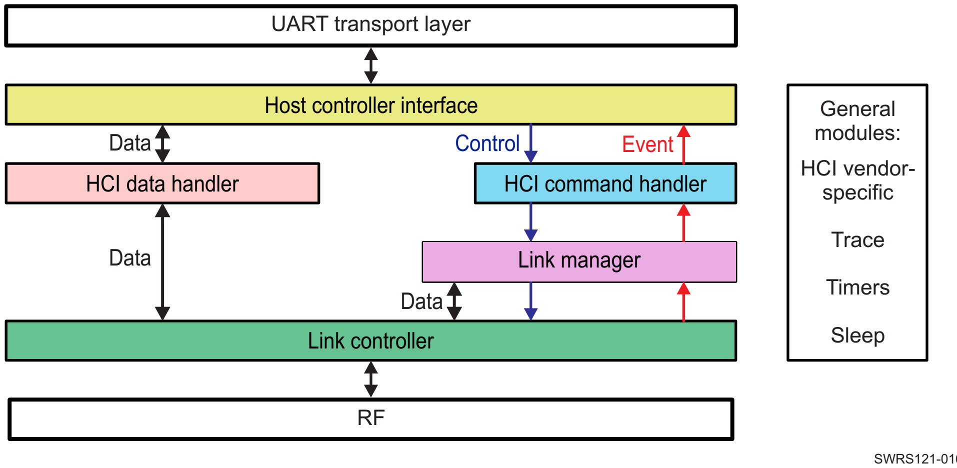


Figure 3-1. *Bluetooth* Transport Layers

PRODUCT PREVIEW

4 Detailed Description

4.1 Terminal Designations

Terminal Functions shows the top view of the terminal designations.

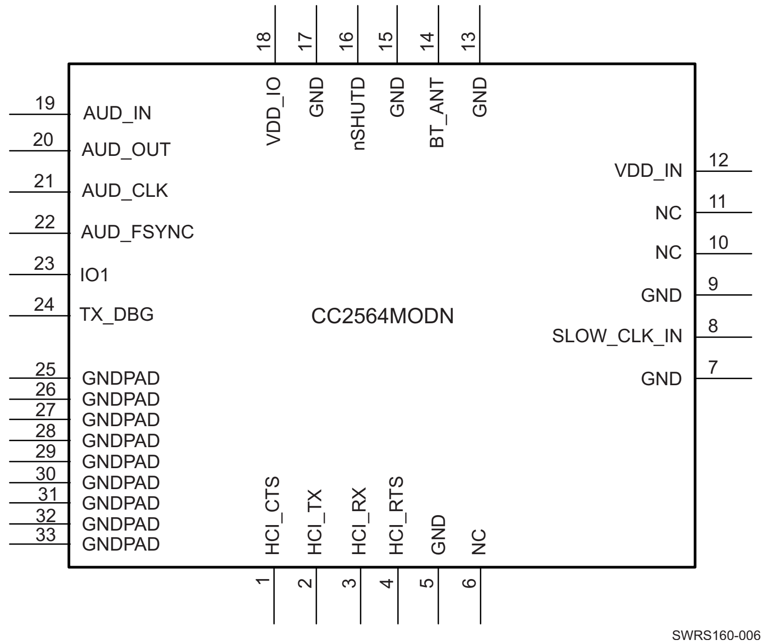


Figure 4-1. Terminal Functions (Top View)

PRODUCT PREVIEW

4.2 Terminal Functions

This section describes the terminal functions.

Table 4-1. Terminal Functions

Name	No.	ESD(1) (V)	Pull at Reset	Def. Dir.(2)	I/O Type(3)	Description	
HCI_CTS	1	750	PU	I	8 mA	HCI UART clear-to-send The device can send data when HCI_CTS is low.	
HCI_TX	2	750	PU	O	8 mA	HCI UART data transmit	
HCI_RX	3	750	PU	I	8 mA	HCI UART data receive	
HCI_RTS	4	750	PU	O	8 mA	HCI UART request-to-send Host can send data when HCI_RTS is low.	
GND	5	1000				Ground	
NC	6			I		Not connected	
GND	7	1000				Ground	
SLOW_CLK_IN	8	1000		I		32.768-kHz clock in	Fail-safe
GND	9	1000				Ground	
NC	10			O		Not connected	
NC	11			O		Not connected	
VDD_IN	12			I		Main power supply for the module	
GND	13					Ground	
BT_ANT	14	500		IO		*Bluetooth* RF I/O	
GND	15					Ground	
nSHUTD	16		PD	I		Shutdown input (active low)	
GND	17					Ground	
VDD_IO	18	1000		I		I/O power supply (1.8 V nominal)	
AUD_IN	19	500	PD	I	4 mA	PCM data input	Fail-safe
AUD_OUT	20	500	PD	O	4 mA	PCM data output	Fail-safe
AUD_CLK	21	500	PD	I/O	HY, 4 mA	PCM clock	Fail-safe
AUD_FSYNC	22	500	PD	I/O	4 mA	PCM frame sync	Fail-safe
IO1	23	500	PD	I/O	4 mA	BT_FUNCT1	
TX_DBG	24	1000	PU	O	2 mA	TI internal debug messages. TI recommends leaving a test point.	
GNDPAD	25	1000				Ground	
GNDPAD	26	1000				Ground	
GNDPAD	27	1000				Ground	
GNDPAD	28	1000				Ground	
GNDPAD	29	1000				Ground	
GNDPAD	30	1000				Ground	
GNDPAD	31	1000				Ground	
GNDPAD	32	1000				Ground	
GNDPAD	33	1000				Ground	

(1) ESD: Human Body Model (HBM). JEDEC 22-A114 2-wire method. CDM: All pins pass 500 V except RF_IO, which passes 400 V.
(2) I = input; O = output; I/O = bidirectional
(3) I/O Type: Digital I/O cells. HY = input hysteresis, current = typical output current

PRODUCT PREVIEW

4.3 Device Power Supply

The power-management hardware and software algorithms of the TI *Bluetooth* HCI module provide significant power savings, which is a critical parameter in an MCU-based system.

The power-management module is optimized for drawing extremely low currents.

4.3.1 Power Sources

The TI *Bluetooth* HCI module requires two power sources:

- VDD_IN: main power supply for the module
- VDD_IO: power source for the 1.8-V I/O ring

The HCI module includes several on-chip voltage regulators for increased noise immunity and can be connected directly to the battery.

4.3.2 Device Power-Up and Power-Down Sequencing

The device includes the following power-up requirements (see Figure 4-2):

- nSHUTD must be low. VDD_IN and VDD_IO are don't-care when nSHUTD is low. However, signals are not allowed on the I/O pins if I/O power is not supplied, because the I/Os are not fail-safe. Exceptions are SLOW_CLK_IN and AUD_xxx, which are fail-safe and can tolerate external voltages with no VDD_IO and VDD_IN.
- VDD_IO and VDD_IN must be stable before releasing nSHUTD.
- The slow clock must be stable within 2 ms of nSHUTD going high.

The device indicates that the power-up sequence is complete by asserting RTS low, which occurs up to 100 ms after nSHUTD goes high. If RTS does not go low, the device is not powered up. In this case, ensure that the sequence and requirements are met.

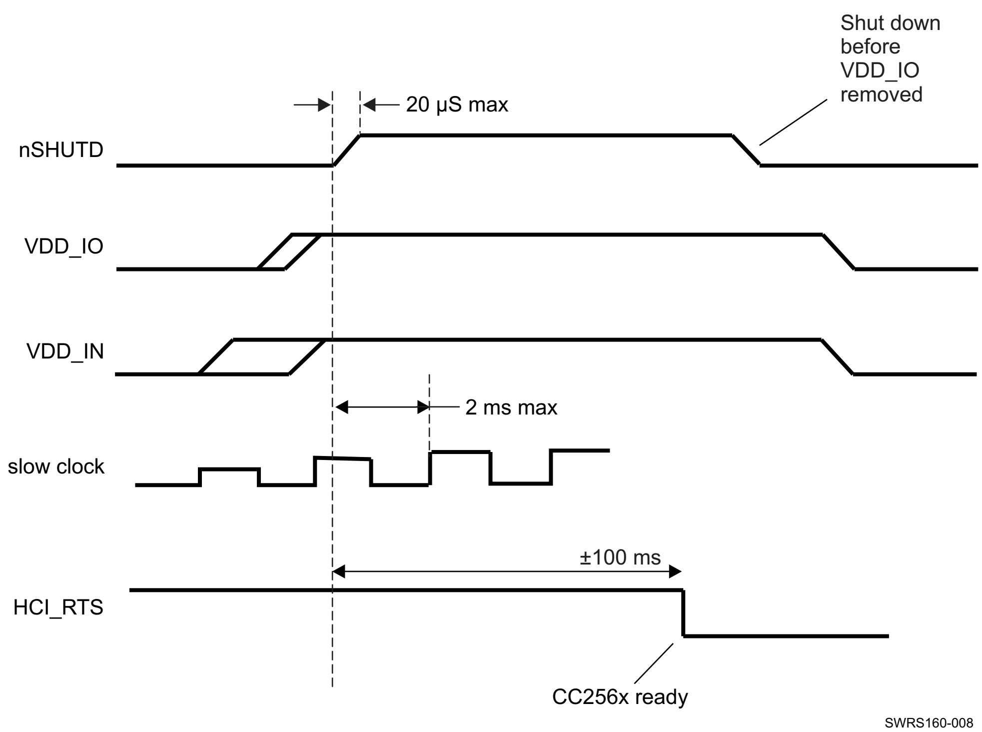


Figure 4-2. Power-Up and Power-Down Sequence

4.3.3 Power Supplies and Shutdown—Static States

The nSHUTD signal puts the device in ultra-low power mode and performs an internal reset to the device. The rise time for nSHUTD must not exceed 20 µs; nSHUTD must be low for a minimum of 5 ms.

To prevent conflicts with external signals, all I/O pins are set to the high-impedance (Hi-Z) state during shutdown and power up of the device. The internal pull resistors are enabled on each I/O pin, as described in Table 4-1. Table 4-2 describes the static operation states.

Table 4-2. Power Modes

	VDD_IN(1)	VDD_IO(1)	nSHUTD(1)	PM_MODE	Comments
1	None	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
2	None	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
3	None	Present	Asserted	Shut down	I/Os are defined as 3-state with internal pullup or pulldown enabled.
4	None	Present	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
5	Present	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
6	Present	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
7	Present	Present	Asserted	Shut down	I/Os are defined as 3-state with internal pullup or pulldown enabled.
8	Present	Present	Deasserted	Active	See Section 4.3.4, *I/O States In Various Power Modes*.

(1) The terms *None* or *Asserted* can imply any of the following conditions: directly pulled to ground or driven low, pulled to ground through a pulldown resistor, or left NC or floating (high-impedance output stage).

4.3.4 I/O States In Various Power Modes

CAUTION

Some device I/Os are not fail-safe (see Section 4.2, *Terminal Functions*). Fail-safe means that the pins do not draw current from an external voltage applied to the pin when I/O power is not supplied to the device. External voltages are not allowed on these I/O pins when the I/O supply voltage is not supplied because of possible damage to the device.

Table 4-3 lists the I/O states in various power modes.

Table 4-3. I/O States in Various Power Modes

I/O Name	Shut Down(1)		Default Active(1)		Deep Sleep(1)	
	I/O State	Pull	I/O State	Pull	I/O State	Pull
HCI_RX	Z	PU	I	PU	I	PU
HCI_TX	Z	PU	O-H	—	O	—
HCI_RTS	Z	PU	O-H	—	O	—
HCI_CTS	Z	PU	I	PU	I	PU
AUD_CLK	Z	PD	I	PD	I	PD
AUD_FSYNC	Z	PD	I	PD	I	PD
AUD_IN	Z	PD	I	PD	I	PD
AUD_OUT	Z	PD	Z	PD	Z	PD
CLK_REQ_OUT	Z	PD	O-H	PD	O-L	PD

(1) I = input, O = output, Z = Hi-Z, — = no pull, PU = pullup, PD = pulldown, H = high, L = low

PRODUCT PREVIEW

Table 4-3. I/O States in Various Power Modes (continued)

I/O Name	Shut Down (1)		Default Active (1)		Deep Sleep (1)	
	I/O State	Pull	I/O State	Pull	I/O State	Pull
IO1	Z	PD	I	PD	I	PD
TX_DBG	Z	PU	O	—		

4.4 Clock Inputs

4.4.1 Slow Clock

An external source must supply the slow clock and connect to the SLOW_CLK_IN pin. The source must be a digital signal in the range of 0 to 1.8 V.

The accuracy of the slow clock frequency must be 32.768 kHz ±250 ppm for *Bluetooth* use (as specified in the *Bluetooth* specification).

The external slow clock must be stable within 64 slow-clock cycles (2 ms) following the release of nSHUTD.

4.5 Functional Blocks

The TI *Bluetooth* HCI module architecture comprises a DRP™ and a point-to-multipoint baseband core. The architecture is based on a single-processor ARM7TDMIE® core. The module includes several on-chip peripherals to enable easy communication with a host system and the *Bluetooth* BR/EDR/LE core.

4.5.1 Host Controller Interface

The TI *Bluetooth* HCI module incorporates one UART module dedicated to the HCI transport layer. The HCI interface transports commands, events, and ACL between the device and the host using HCI data packets.

The maximum baud rate of the UART module is 4 Mbps; however, the default baud rate after power up is set to 115.2 kbps. The baud rate can thereafter be changed with a VS command. The device responds with a command complete event (still at 115.2 kbps), after which the baud rate change occurs.

The UART module includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTS and RTS hardware flow control (H4 protocol)
- XON and XOFF software flow control (H5 protocol)

Table 4-4 lists the UART module default settings.

Table 4-4. UART Module Default Settings

Parameter	Value
Bit rate	115.2 kbps
Data length	8 bits
Stop bit	1
Parity	None

4.5.1.1 H4 Protocol—4-Wire UART Interface

The H4 UART interface includes four signals:

- TX
- RX

PRODUCT PREVIEW

- CTS
- RTS

Flow control between the host and the TI *Bluetooth* HCI module is bytewise by hardware.

Figure 4-3 shows the H4 UART interface.

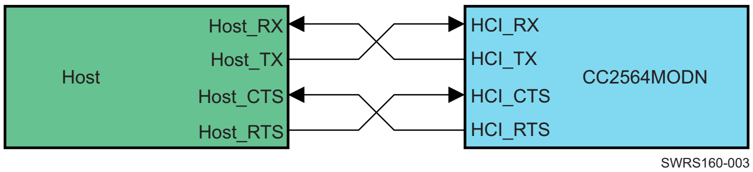


Figure 4-3. H4 UART Interface

When the UART RX buffer of the TI *Bluetooth* HCI module passes the flow control threshold, it sets the HCI_RTS signal high to stop transmission from the host.

When the HCI_CTS signal is set high, the module stops transmission on the interface. If HCI_CTS is set high while transmitting a byte, the module finishes transmitting the byte and stops the transmission.

The H4 protocol device includes a mechanism that handles the transition between active mode and sleep mode. The protocol occurs through the CTS and RTS UART lines and is known as the enhanced HCI low level (eHCILL) power-management protocol.

For more information on the H4 UART protocol, see *Volume 4 Host Controller Interface, Part A UART Transport Layer of the Bluetooth Core Specifications* (www.bluetooth.org/en-us/specification/adoptedspecifications).

4.5.1.2 H5 Protocol—3-Wire UART Interface

The H5 UART interface consists of three signals (see Figure 4-4):

- TX
- RX
- GND

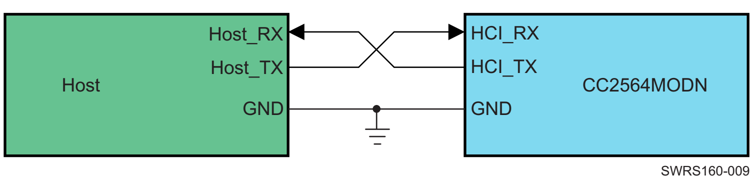


Figure 4-4. H5 UART Interface

The H5 protocol supports the following features:

- Software flow control (XON/XOFF)
- Power management using the software messages:
  - WAKEUP
  - WOKEN
  - SLEEP
- CRC data integrity check

For more information on the H5 UART protocol, see *Volume 4 Host Controller Interface, Part D Three-Wire UART Transport Layer of the Bluetooth Core Specifications* (www.bluetooth.org/en-us/specification/adoptedspecifications).

PRODUCT PREVIEW

PRODUCT PREVIEW

4.5.2 Digital Codec Interface

The codec interface is a fully programmable port to support seamless interfacing with different PCM and I2S codec devices. The interface includes the following features:

- Two voice channels
- Master and slave modes
- All voice coding schemes defined by the *Bluetooth* specification: linear, A-Law, and μ-Law
- Long and short frames
- Different data sizes, order, and positions
- High flexibility to support a variety of codecs
- Bus sharing: Data_Out is in Hi-Z state when the interface is not transmitting voice data.

4.5.2.1 Hardware Interface

The interface includes four signals:

- Clock: configurable direction (input or output)
- Frame_Sync and Word_Sync: configurable direction (input or output)
- Data_In: input
- Data_Out: output or 3-state

The module can be the master of the interface when generating the Clock and Frame_Sync signals or the slave when receiving these two signals.

For slave mode, clock input frequencies of up to 15 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits.

For master mode, the module can generate any clock frequency between 64 kHz and 4.096 MHz.

4.5.2.2 I2S

When the codec interface is configured to support the I2S protocol, these settings are recommended:

- Bidirectional, full-duplex interface
- Two time slots per frame: time slot-0 for the left channel audio data; and time slot-1 for the right channel audio data
- Each time slot is configurable up to 40 serial clock cycles long, and the frame is configurable up to 80 serial clock cycles long.

4.5.2.3 Data Format

The data format is fully configurable:

- The data length can be from 8 to 320 bits in 1-bit increments when working with 2 channels, or up to 640 bits when working with 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable within 1 clock (bit) resolution and can be set independently (relative to the edge of the Frame_Sync signal) for each channel.
- The Data_In and Data_Out bit order can be configured independently. For example; Data_In can start with the most significant bit (MSB); Data_Out can start with the least significant bit (LSB). Each channel is separately configurable. The inverse bit order (that is, LSB first) is supported only for sample sizes up to 24 bits.
- Data_In and Data_Out are not required to be the same length.
- The Data_Out line is configured to Hi-Z output between data words. Data_Out can also be set for permanent Hi-Z, regardless of the data output. This configuration allows the module to be a bus slave in a multislave PCM environment. At power up, Data_Out is configured as Hi-Z.

4.5.2.4 Frame Idle Period

The codec interface handles frame idle periods, in which the clock pauses and becomes 0 at the end of the frame, after all data are transferred.

The module supports frame idle periods both as master and slave of the codec bus.

When the module is the master of the interface, the frame idle period is configurable. There are two configurable parameters:

- Clk_Idle_Start: indicates the number of clock cycles from the beginning of the frame to the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock becomes 0.
- Clk_Idle_End: indicates the time from the beginning of the frame to the end of the idle period. The time is given in multiples of clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

For example, for clock rate = 1 MHz, frame sync period = 10 kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90.

Between both Frame_Sync signals there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and lasts 90 – 60 = 30 clock cycles. Thus, the idle period ends 100 – 90 = 10 clock cycles before the end of the frame. The data transmission must end before the beginning of the idle period.

Figure 4-5 shows the frame idle timing.

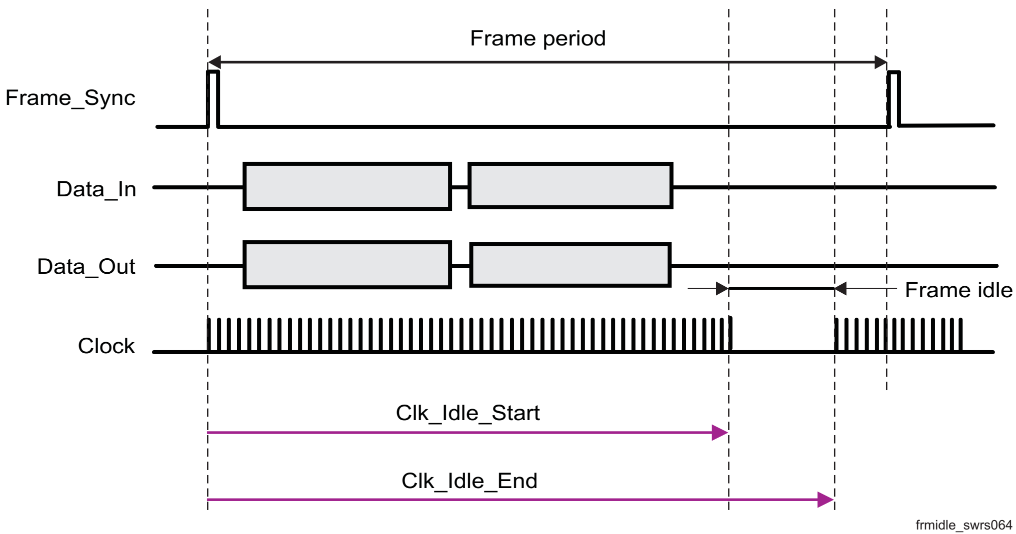


Figure 4-5. Frame Idle Period

4.5.2.5 Clock-Edge Operation

The codec interface of the module can work on the rising or the falling edge of the clock and can sample the Frame_Sync signal and the data at inversed polarity.

Figure 4-6 shows the operation of a falling-edge-clock type of codec. The codec is the master of the bus. The Frame_Sync signal is updated (by the codec) on the falling edge of the clock and is therefore sampled (by the module) on the next rising clock. The data from the codec is sampled (by the module) on the falling edge of the clock.

PRODUCT PREVIEW

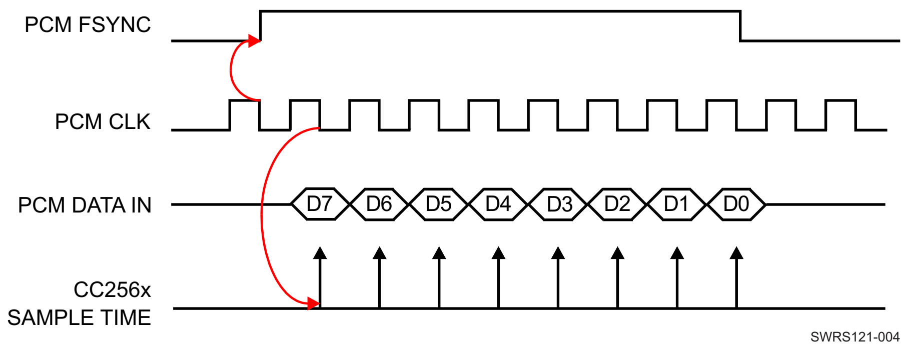


Figure 4-6. Negative Clock Edge Operation

4.5.2.6 Two-Channel Bus Example

Figure 4-7 shows a 2-channel bus in which the two channels have different word sizes and arbitrary positions in the bus frame. (FT stands for frame timer.)

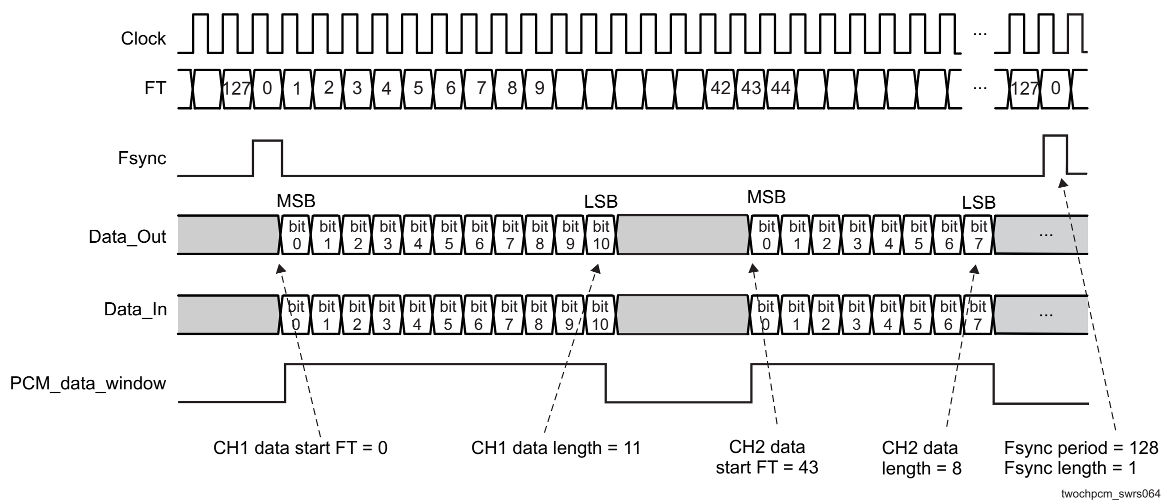


Figure 4-7. 2-Channel Bus Timing

4.5.2.7 Improved Algorithm For Lost Packets

The module features an improved algorithm to improve voice quality when received voice data packets are lost. There are two options:

- Repeat the last sample: possible only for sample sizes up to 24 bits. For sample sizes larger than 24 bits, the last byte is repeated.
- Repeat a configurable sample of 8 to 24 bits (depending on the real sample size) to simulate silence (or anything else) in the bus. The configured sample is written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.

4.5.2.8 *Bluetooth* and Codec Clock Mismatch Handling

In *Bluetooth* RX, the module receives RF voice packets and writes them to the codec interface. If the module receives data faster than the codec interface output allows, an overflow occurs. In this case, the *Bluetooth* has two possible modes of behavior:

- Allow overflow: if overflow is allowed, the *Bluetooth* continues receiving data and overwrites any data not yet sent to the codec.
- Do not allow overflow: if overflow is not allowed, RF voice packets received when the buffer is full are discarded.

PRODUCT PREVIEW

4.5.3 Assisted Modes

The TI *Bluetooth* HCI module contains an embedded coprocessor (see Figure 1-1) that can be used for multiple purposes. The module uses the coprocessor to perform the LE or ANT functionality. The The module also uses the coprocessor to execute the assisted HFP 1.6 (WBS) or assisted A2DP functions. Only one of these functions can be executed at a time because they all use the same resources (that is, the coprocessor; see Table 3-1 for the modes of operation supported by the module).

This section describes the assisted HFP 1.6 (WBS) and assisted A2DP modes of operation in the module. These modes of operation minimize host processing and power by taking advantage of the device coprocessor to perform the voice and audio SBC processing required in HFP 1.6 (WBS) and A2DP profiles. This section also compares the architecture of the assisted modes with the common implementation of the HFP 1.6 and A2DP profiles.

The assisted HFP 1.6 (WBS) and assisted A2DP modes of operation comply fully with the HFP 1.6 and A2DP *Bluetooth* specifications. For more information on these profiles, see the corresponding *Bluetooth* Profile Specification (www.bluetooth.org/en-us/specification/adopted-specifications).

4.5.3.1 Assisted HFP 1.6 (WBS)

The *HFP 1.6 Profile Specification* adds the requirement for WBS support. The WBS feature allows twice the voice quality versus legacy voice coding schemes at the same air bandwidth (64 kbps). This feature is achieved using a voice sampling rate of 16 kHz, a modified subband coding (mSBC) scheme, and a packet loss concealment (PLC) algorithm. The mSBC scheme is a modified version of the mandatory audio coding scheme used in the A2DP profile with the parameters listed in Table 4-5.

Table 4-5. mSBC Parameters

Parameter	Value
Channel mode	Mono
Sampling rate	16 kHz
Allocation method	Loudness
Subbands	8
Block length	15
Bitpool	26

The assisted HFP 1.6 mode of operation implements this WBS feature on the embedded coprocessor. That is, the mSBC voice coding scheme and the PLC algorithm are executed in the coprocessor rather than in the host, thus minimizing host processing and power. One WBS connection at a time is supported and WBS and NBS connections cannot be used simultaneously in this mode of operation. Figure 4-8 shows the architecture comparison between the common implementation of the HFP 1.6 profile and the assisted HFP 1.6 solution.

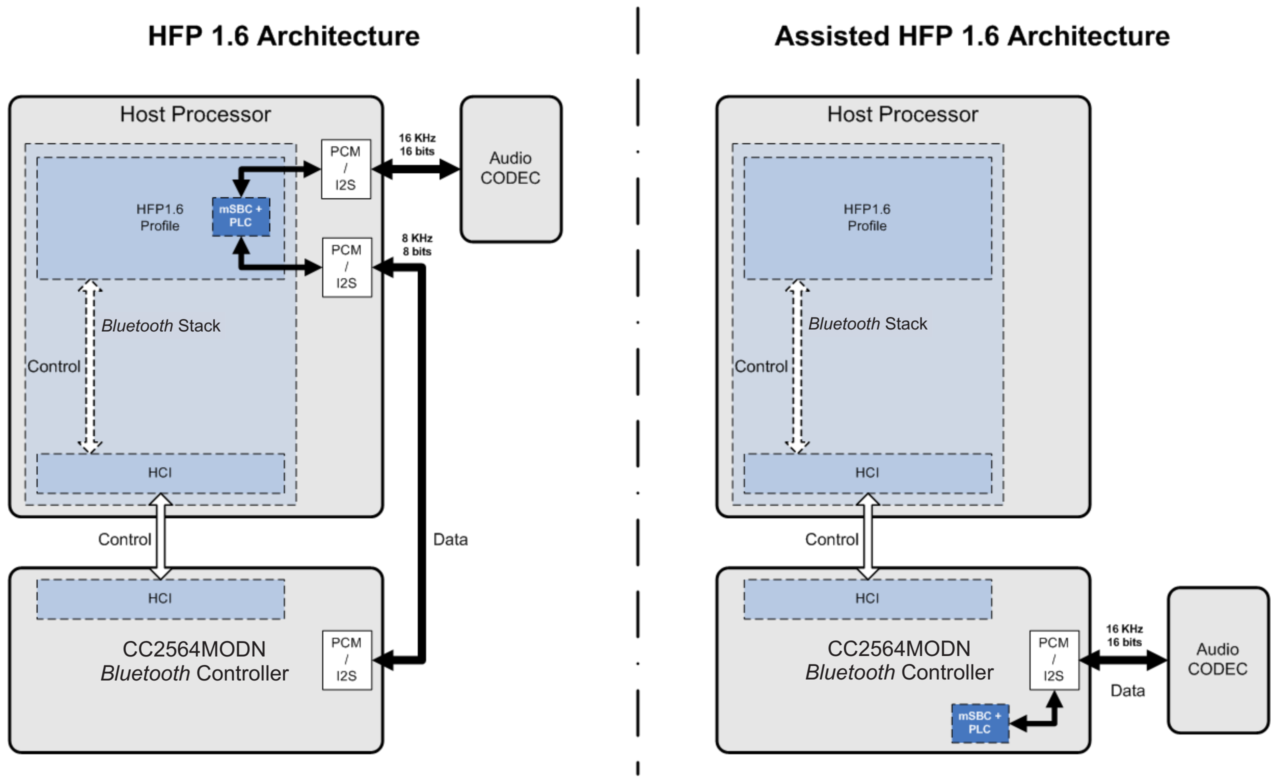


Figure 4-8. HFP 1.6 Architecture Versus Assisted HFP 1.6 Architecture

For detailed information on the HFP 1.6 profile, see the *Hands-Free Profile 1.6 Specification* (www.bluetooth.org/en-us/specification/adopted-specifications).

4.5.3.2 Assisted A2DP

The A2DP enables wireless transmission of high-quality mono or stereo audio between two devices. A2DP defines two roles:

- A2DP source is the transmitter of the audio stream.
- A2DP sink is the receiver of the audio stream.

A typical use case streams music from a tablet, phone, or PC (the A2DP source) to headphones or speakers (the A2DP sink). This section describes the architecture of these roles and compares them with the corresponding assisted-A2DP architecture. To use the air bandwidth efficiently, the audio data must be compressed in a proper format. The A2DP mandates support of the SBC scheme. Other audio coding algorithms can be used; however, both *Bluetooth* devices must support the same coding scheme. SBC is the only coding scheme spread out in all A2DP *Bluetooth* devices, and thus the only coding scheme supported in the assisted A2DP modes. Table 4-6 lists the recommended parameters for the SBC scheme in the assisted A2DP modes.

Table 4-6. Recommended Parameters for the SBC Scheme in Assisted A2DP Modes

SBC Encoder Settings(1)	Mid Quality				High Quality			
	Mono		Joint Stereo		Mono		Joint Stereo	
Sampling frequency (kHz)	44.1	48	44.1	48	44.1	48	44.1	48
Bitpool value	19	18	35	33	31	29	53	51
Resulting frame length (bytes)	46	44	83	79	70	66	119	115
Resulting bit rate (Kbps)	127	132	229	237	193	198	328	345

(1) Other settings: Block length = 16; allocation method = loudness; subbands = 8.

The SBC scheme supports a wide variety of configurations to adjust the audio quality. Table 4-7 through Table 4-14 list the supported SBC capabilities in the assisted A2DP modes.

Table 4-7. Channel Modes

Channel Mode	Status
Mono	Supported
Stereo	Supported
Joint stereo	Supported

Table 4-8. Sampling Frequency

Sampling Frequency (kHz)	Status
16	Supported
44.1	Supported
48	Supported

Table 4-9. Block Length

Block Length	Status
16	Supported

Table 4-10. Subbands

Subbands	Status
8	Supported

Table 4-11. Allocation Method

Allocation Method	Status
Loudness	Supported

Table 4-12. Bitpool Values

Bitpool Range	Status
Assisted A2DP sink: TBD	Supported
Assisted A2DP source: 2–57	Supported

PRODUCT PREVIEW

Table 4-13. L2CAP MTU Size

L2CAP MTU Size (Bytes)	Status
Assisted A2DP sink: 260–800	Supported
Assisted A2DP source: 260–1021	Supported

Table 4-14. Miscellaneous Parameters

Item	Value	Status
A2DP content protection	Protected	Not supported
AVDTP service	Basic type	Supported
L2CAP mode	Basic mode	Supported
L2CAP flush	Nonflushable	Supported

For detailed information on the A2DP profile, see the *A2DP Profile Specification* (www.bluetooth.org/enus/specification/adopted-specifications).

4.5.3.2.1 Assisted A2DP Sink

The A2DP sink role is the receiver of the audio stream in an A2DP *Bluetooth* connection. In this role, the A2DP layer and its underlying layers are responsible for link management and data decoding. To handle these tasks, two logic transports are defined:

- Control and signaling logic transport
- Data packet logic transport

The assisted A2DP takes advantage of this modularity to handle the data packet logic transport in the module by implementing a light L2CAP layer (L-L2CAP) and light AVDTP layer (L-AVDTP) to defragment the packets. Then the assisted A2DP performs the SBC decoding on-chip to deliver raw audio data through the module PCM–I2S interface. Figure 4-9 shows the comparison between a common A2DP sink architecture and the assisted A2DP sink architecture.

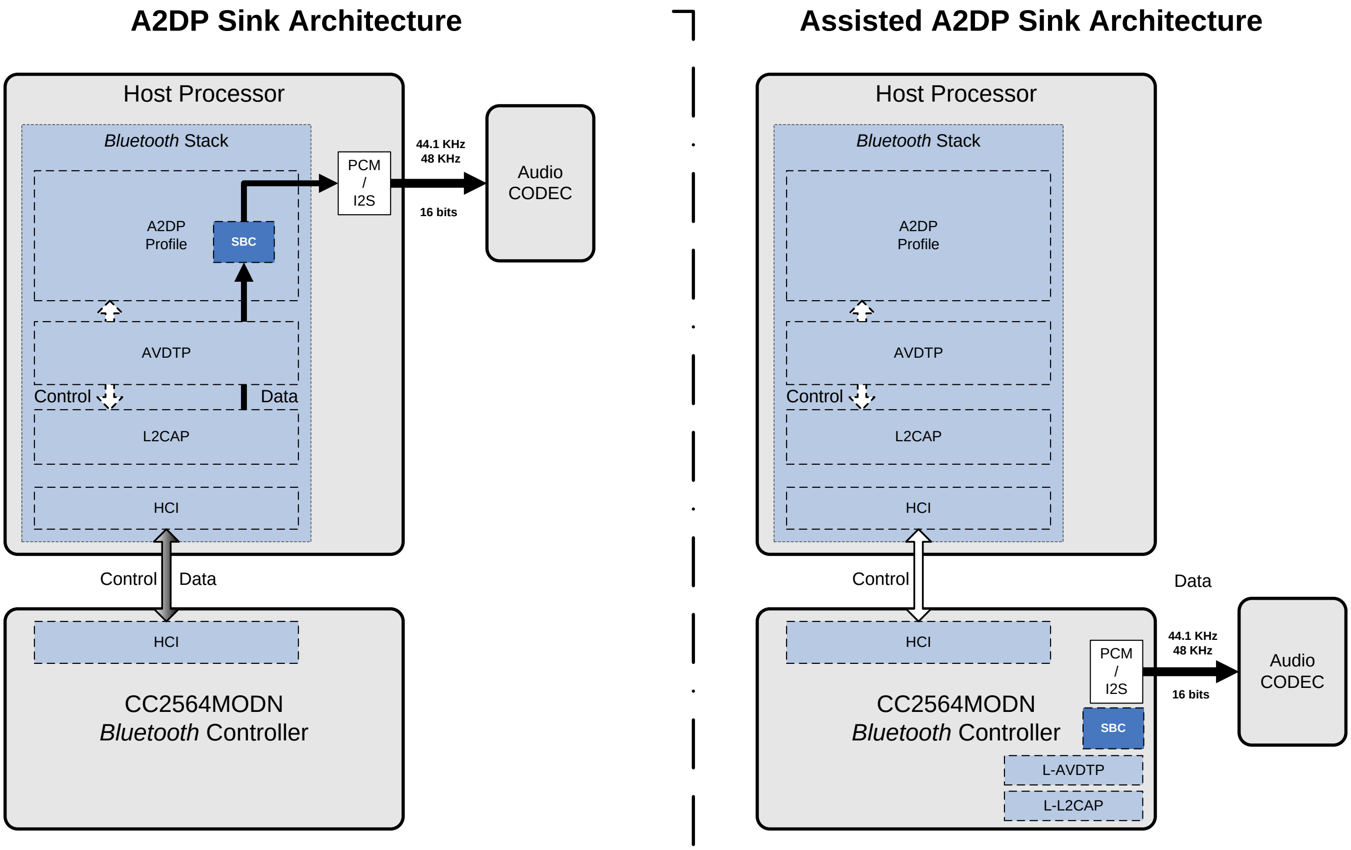


Figure 4-9. A2DP Sink Architecture Versus Assisted A2DP Sink Architecture

For more information on the A2DP sink role, see the *A2DP Profile Specification* (www.bluetooth.org/enus/specification/adopted-specifications).

4.5.3.2.2 Assisted A2DP Source

The role of the A2DP source is to transmit the audio stream in an A2DP *Bluetooth* connection. In this role, the A2DP layer and its underlying layers are responsible for link management and data encoding. To handle these tasks, two logic transports are defined:

- Control and signaling logic transport
- Data packet logic transport

The assisted A2DP takes advantage of this modularity to handle the data packet logic transport in the module. First, the assisted A2DP encodes the raw data from the module PCM–I2S interface using an on-chip SBC encoder. The assisted A2DP then implements an L-L2CAP layer and an L-AVDTP layer to fragment and packetize the encoded audio data. Figure 4-10 shows the comparison between a common A2DP source architecture and the assisted A2DP source architecture.

PRODUCT PREVIEW

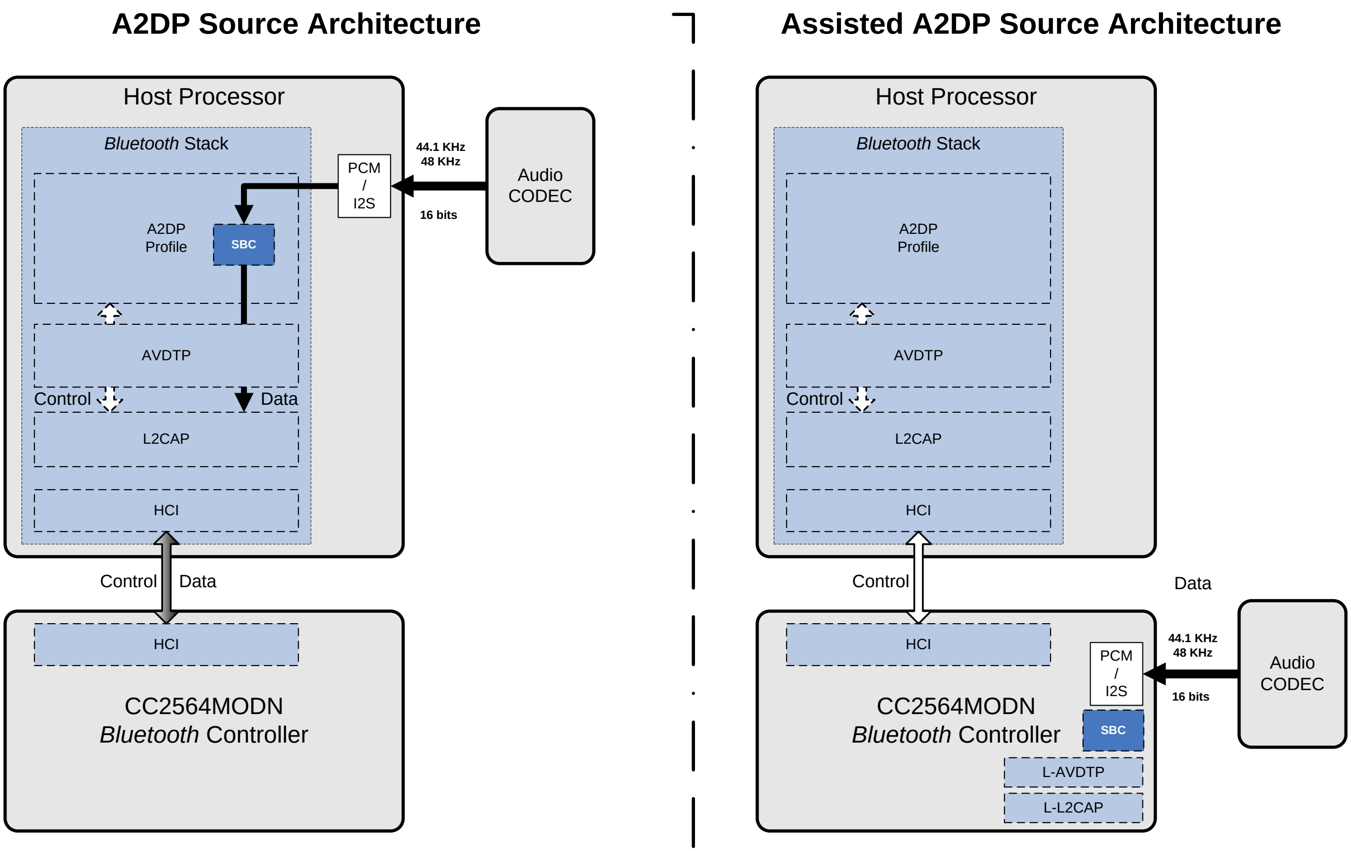


Figure 4-10. A2DP Source Architecture Versus Assisted A2DP Source Architecture

For more information on the A2DP source role, see the *A2DP Profile Specification* (www.bluetooth.org/enus/ specification/adopted-specifications).

PRODUCT PREVIEW

5 Device Specifications

Unless otherwise indicated, all measurements are taken at the device pins of the TI test evaluation board (EVB). All specifications are over process, voltage, and temperature, unless otherwise indicated.

5.1 General Device Requirements and Operation

5.1.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise indicated)

NOTE

Unless otherwise indicated, all parameters are measured as follows:

VDD_IN = 3.6 V, VDD_IO = 1.8 V

Parameters (1)		Value	Unit
Ratings over operating free-air temperature range			
VDD_IN	Supply voltage range	–0.5 to 4.8	V (2)
VDD_IO		–0.5 to 2.145	V
	Input voltage to analog pins (3)	–0.5 to 2.1	V
	Input voltage to all other pins	–0.5 to (VDD_IO + 0.5)	V
	Operating ambient temperature range (4)	–40 to 85	°C
	Bluetooth RF inputs	10	dBm

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum allowed depends on accumulated time at that voltage: VDD_IN is defined in Section 6, *Reference Design for Power and Radio Connections*.
(3) Analog pins: BT_RF, XTALP, and XTALM
(4) The reference design supports a temperature range of –20°C to 70°C because of the operating conditions of the crystal.

5.2 Handling Ratings

			VALUE	UNIT
T_{stg}	Storage temperature range		–55 to 125	°C
ESD stress voltage (1)	Human body model (HBM) (2)	Device	TBD	V
	Charged device model (CDM) (3)	Device	TBD	

(1) ESD measures device sensitivity and immunity to damage caused by electrostatic discharges into the device.
(2) The level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible, if necessary precautions are taken. Pins listed as 1000 V can actually have higher performance.
(3) The level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible, if necessary precautions are taken. Pins listed as 250 V can actually have higher performance.

5.2.1 Recommended Operating Conditions

Rating	Condition	Sym	Min	Max	Unit
Power supply voltage		VDD_IN	2.2	4.8	V
I/O power supply voltage		VDD_IO	1.62	1.92	V
High-level input voltage	Default	V_{IH}	0.65 x VDD_IO	VDD_IO	V
Low-level input voltage	Default	V_{IL}	0	0.35 x VDD_IO	V
I/O input rise and all times,10% to 90% — asynchronous mode		t_r and t_f	1	10	ns
I/O input rise and fall times, 10% to 90% — synchronous mode (PCM)			1	2.5	ns
Voltage dips on VDD_IN (V_{BAT}) duration = 577 µs to 2.31 ms, period = 4.6 ms				400	mV

PRODUCT PREVIEW

Rating	Condition	Sym	Min	Max	Unit
Maximum ambient operating temperature(1) (2)			–20	70	°C

(1) The device can be reliably operated for 7 years at $T_{ambient}$ of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).
(2) A crystal-based solution is limited by the temperature range required of the crystal to meet 20 ppm.

5.2.2 Current Consumption

5.2.2.1 Static Current Consumption

Operational Mode	Min	Typ	Max	Unit
Shutdown mode(1)		1	7	µA
Deep sleep mode(2)		40	105	µA
Total I/O current consumption in active mode			1	mA
Continuous transmission—GFSK(3)			107	mA
Continuous transmission—EDR(4)(5)			112.5	mA

(1) $V_{BAT} + V_{IO} + V_{SHUTDOWN}$
(2) $V_{BAT} + V_{IO}$
(3) At maximum output power (10 dBm)
(4) At maximum output power (8 dBm)
(5) Both π/4 DQPSK and 8DPSK

5.2.2.2 Dynamic Current Consumption

5.2.2.2.1 Current Consumption for Different Bluetooth BR/EDR Scenarios

Conditions: VDD_IN = 3.6 V, 25°C, nominal unit, 8-dBm output power

Operational Mode	Master and Slave	Average Current	Unit
Synchronous connection oriented (SCO) link HV3	Master and slave	13.7	mA
Extended SCO (eSCO) link EV3 64 kbps, no retransmission	Master and slave	13.2	mA
eSCO link 2-EV3 64 kbps, no retransmission	Master and slave	10	mA
GFSK full throughput: TX = DH1, RX = DH5	Master and slave	40.5	mA
EDR full throughput: TX = 2-DH1, RX = 2-DH5	Master and slave	41.2	mA
EDR full throughput: TX = 3-DH1, RX = 3-DH5	Master and slave	41.2	mA
Sniff, four attempts, 1.28 seconds	Master and slave	145	µA
Page or inquiry scan 1.28 seconds, 11.25 ms	Master and slave	320	µA
Page (1.28 seconds) and inquiry (2.56 seconds) scans, 11.25 ms	Master and slave	445	µA
A2DP source	Master	13.9	mA
A2DP sink	Master	15.2	mA
A3DP source	Master	16.9	mA
A3DP sink	Master	18.1	mA
Assisted WBS EV3; retransmit effort = 2; maximum latency = 8 ms	Master and slave	17.5 and 18.5	mA
Assisted WBS 2EV3; retransmit effort = 2; maximum latency = 12 ms	Master and slave	11.9 and 13	mA

PRODUCT PREVIEW

5.2.2.2.2 Current Consumption for Different LE Scenarios

Conditions: VDD_IN = 3.6 V, 25°C, nominal unit, 8-dBm output power

Mode	Description	Average Current	Unit
Advertising, nonconnectable	Advertising in all three channels 1.28-seconds advertising interval 15 bytes advertise data	114	µA
Advertising, discoverable	Advertising in all three channels 1.28-seconds advertising interval 15 bytes advertise data	138	µA
Scanning	Listening to a single frequency per window 1.28-seconds scan interval 11.25-ms scan window	324	µA
Connected (master and slave role)	500-ms connection interval 0-ms slave connection latency Empty TX and RX LL packets	169 and 199 (master and slave)	µA

5.2.3 General Electrical Characteristics

Rating			Condition	Min	Max	Unit
High-level output voltage, V_{OH}			At 2, 4, 8 mA	0.8 x VDD_IO	VDD_IO	V
			At 0.1 mA	VDD_IO – 0.2	VDD_IO	
Low-level output voltage, V_{OL}			At 2, 4, 8 mA	0	0.2 x VDD_IO	V
			At 0.1 mA	0	0.2	
I/O input impedance			Resistance	1		MΩ
			Capacitance		5	pF
Output rise and fall times, 10% to 90% (digital pins)			C_L = 20 pF		10	ns
I/O pull currents	PCM-I2S bus, TX_DBG	PU	typ = 6.5	3.5	9.7	µA
		PD	typ = 27	9.5	55	
	All others	PU	typ = 100	50	300	µA
		PD	typ = 100	50	360	

5.2.4 nSHUTD Requirements

Parameter	Sym	Min	Max	Unit
Operation mode level (1)	V_{IH}	1.42	1.98	V
Shutdown mode level (1)	V_{IL}	0	0.4	V
Minimum time for nSHUT_DOWN low to reset the device		5		ms
Rise and fall times	t_r and t_f		20	µs

(1) An internal 300-kΩ pulldown retains shut-down mode when no external signal is applied to this pin.

PRODUCT PREVIEW

5.2.5 Slow Clock Requirements

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy (Initial + temp + aging)	*Bluetooth*				±250	ppm
	ANT				±50	
Input transition time t_r and t_f (10% to 90%)		t_r and t_f			200	ns
Frequency input duty cycle			15%	50%	85%	
Slow clock input voltage limits	Square wave, DC-coupled	V_{IH}	0.65 × VDD_IO		VDD_IO	V peak
		V_{IL}	0		0.35 × VDD_IO	V peak
Input impedance			1			MΩ
Input capacitance					5	pF

5.3 *Bluetooth* BR/EDR RF Performance

All parameters in this section that are fast-clock dependent are verified using a 38.4-MHz XTAL and an RF load of 50 Ω at the BT_RF port.

5.3.1 Bluetooth Receiver—In-Band Signals

Characteristics	Condition	Min	Typ	Max	*Bluetooth* Specification	Unit
Operation frequency range		2402		2480		MHz
Channel spacing			1			MHz
Input impedance			50			Ω
Sensitivity, dirty TX on(1)	GFSK, BER = 0.1%		–93		–70	dBm
	Pi/4-DQPSK, BER = 0.01%		–92.5		–70	
	8DPSK, BER = 0.01%		–85.5		–70	
BER error floor at sensitivity + 10 dB, dirty TX off	Pi/4-DQPSK		1E–7		1E–5	
	8DPSK				1E–5	
Maximum usable input power	GFSK, BER = 0.1%	–5			–20	dBm
	Pi/4-DQPSK, BER = 0.1%	–10				
	8DPSK, BER = 0.1%	–10				
Intermodulation characteristics	Level of interferers (for n = 3, 4, and 5)		–30		–39	dBm

PRODUCT PREVIEW

(1) Sensitivity degradation up to 3 dB may occur for minimum and typical values where the *Bluetooth* frequency is a harmonic of the fast clock.

Characteristics	Condition		Min	Typ	Max	*Bluetooth* Specification	Unit
C/I performance[(2)] Image = –1 MHz	GFSK, co-channel			8		11	dB
	EDR, co-channel	Pi/4-DQPSK		9.5		13	
		8DPSK		16.5		21	
	GFSK, adjacent ±1 MHz			–10		0	
	EDR, adjacent ±1 MHz, (image)	Pi/4-DQPSK		–10		0	
		8DPSK		–5		5	
	GFSK, adjacent +2 MHz			–38		–30	
	EDR, adjacent, +2 MHz	Pi/4-DQPSK		–38		–30	
		8DPSK		–38		–25	
	GFSK, adjacent –2 MHz			–28		–20	
	EDR, adjacent –2 MHz	Pi/4-DQPSK		–28		–20	
		8DPSK		–22		–13	
	GFSK, adjacent ≥ |±3| MHz			–45		–40	
	EDR, adjacent ≥ |±3| MHz	Pi/4-DQPSK		–45		–40	
		8DPSK		–44		–33	
RF return loss				–10			dB
RX mode LO leakage	Frf = (received RF – 0.6 MHz)			–63			dBm

(2) Numbers show ratio of desired signal to interfering signal. Smaller numbers indicate better C/I performance.

5.3.2 Bluetooth Transmitter—GFSK

Characteristics	Min	Typ	Max	*Bluetooth* Specification	Unit
Maximum RF output power[(1)]		10			dBm
Gain control range		30			dB
Power control step	2		8	2 to 8	
Adjacent channel power |M–N| = 2		–45		≤ –20	dBm
Adjacent channel power |M–N| > 2		–50		≤ –40	

(1) To modify maximum output power, use an HCI VS command.

5.3.3 Bluetooth Transmitter—EDR

Characteristics			Min (25°C, –40°C, 85°C)	Typ (25°C, –40°C, 85°C)	Max (25°C, –40°C, 85°C)	*Bluetooth* Specification	Unit
EDR output power	Pi/4-DQPSK	VDD_IN = V_{BAT}		8			dBm
	8DPSK	VDD_IN = V_{BAT}		8			
EDR relative power			–2		1	–4 to +1	dB
Gain control range				30			
Power control step			2		8	2 to 8	
Adjacent channel power |M–N| = 1				–30		≤ –26	dBc
Adjacent channel power |M–N| = 2				–27		≤ –20	dBm
Adjacent channel power |M–N| > 2 [(1)]				–42		≤ –40	dBm

(1) Adjacent channel power measurements take into account specification exception of three bands, as defined by the *Test Suite Structure (TSS) and Test Purposes (TP) Bluetooth Documentation Specification*.

PRODUCT PREVIEW

5.3.4 Bluetooth Modulation—GFSK

Characteristics	Condition		Sym	Min	Typ	Max	*Bluetooth* Specification	Unit
–20 dB bandwidth	GFSK				925		≤ 1000	kHz
Modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 111100001111...	F1 avg		165		140 to 175	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	F2 max		130		> 115	kHz
	Δf2avg, Δf1avg				88		> 80	%
Absolute carrier frequency drift	DH1			–25		25	< ±25	kHz
	DH3 and DH5			–35		35	< ±40	
Drift rate						20	< 20	kHz/ 50 µs
Initial carrier frequency tolerance	f0 – fTX			–75		+75	< ±75	kHz

5.3.5 Bluetooth Modulation—EDR

Characteristics	Condition	Min	Typ	Max	*Bluetooth* Specification	Unit
Carrier frequency stability		–10		10	≤ 10	kHz
Initial carrier frequency tolerance		–75		75	±75	kHz
Rms DEVM [(1)]	Pi/4-DQPSK		6		20	%
	8DPSK		6		13	
99% DEVM [(1)]	Pi/4-DQPSK			30	30	
	8DPSK			20	20	
Peak DEVM [(1)]	Pi/4-DQPSK		14		35	
	8DPSK		16		25	

(1) Max performance refers to maximum TX power.

5.4 *Bluetooth* LE RF Performance

All parameters in this section that are fast-clock dependent are verified using a 38.4-MHz XTAL and an RF load of 50 Ω at the BT_RF port.

5.4.1 BLE Receiver—In-Band Signals

Characteristic	Condition	Min	Typ	Max	BLE Specification	Unit
Operation frequency range		2402		2480		MHz
Channel spacing			2			MHz
Input impedance			50			Ω
Sensitivity, dirty TX on [(1)]	PER = 30.8%; dirty TX on		–93		≤ –70	dBm
Maximum usable input power	GMSK, PER = 30.8%	–10			≥ –10	dBm
Intermodulation characteristics	Level of interferers (for n = 3, 4, 5)		–30		≥ –50	dBm

(1) Sensitivity degradation up to 3 dB may occur where the BLE frequency is a harmonic of the fast clock.

Characteristic	Condition	Min	Typ	Max	BLE Specification	Unit
C/I performance(2) Image = –1 MHz	GMSK, co-channel		8		≤ 21	dB
	GMSK, adjacent ±1 MHz		–5		≤ 15	
	GMSK, adjacent +2 MHz		–45		≤ –17	
	GMSK, adjacent –2 MHz		–22		≤ –15	
	GMSK, adjacent ≥ |±3| MHz		–47		≤ –27	
RX mode LO leakage	Frf = (received RF – 0.6 MHz)		–63			dBm

(2) Numbers show wanted signal-to-interfering signal ratio. Smaller numbers indicate better C/I performance.

5.4.2 BLE Transmitter

Characteristics	Min	Typ	Max	BLE Specification	Unit
RF output power (VDD_IN = VBAT)(1)		10(2)		≤10	dBm
Adjacent channel power |M-N| = 2		–45		≤ –20	dBm
Adjacent channel power |M-N| > 2		–50		≤ –30	

(1) To modify maximum output power, use an HCI VS command.
(2) To achieve the BLE specification of 10-dBm maximum, an insertion loss of > 2 dB is assumed between the RF ball and the antenna. Otherwise, use an HCI VS command to modify the output power.

5.4.3 BLE Modulation

Characteristics	Condition		Sym	Min	Typ	Max	BLE Specification	Unit
Modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 111100001111000 0...	Δf1 avg		250		225 to 275	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	Δf2 max		210		≥ 185	kHz
	Δf2avg, Δf1avg				0.9		≥ 0.8	
Absolute carrier frequency drift				–25		25	≤ ±50	kHz
Drift rate						15	≤ 20	kHz/50 ms
Initial carrier frequency tolerance				–25		25	≤ ±100	kHz

5.5 Interface Specifications

5.5.1 UART

Figure 5-1 shows the UART timing diagram. Table 5-1 lists the UART timing characteristics.

PRODUCT PREVIEW

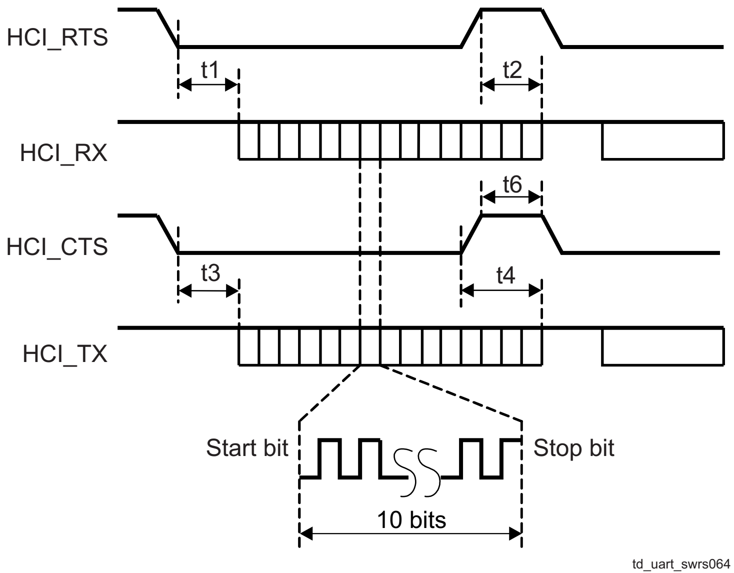


Figure 5-1. UART Timing

PRODUCT PREVIEW

Table 5-1. UART Timing Characteristics

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
	Baud rate		37.5		4000	kbps
	Baud rate accuracy per byte	Receive and transmit	–2.5		1.5	%
	Baud rate accuracy per bit	Receive and transmit	–12.5		12.5	%
t3	CTS low to TX_DATA on		0	2		µs
t4	CTS high to TX_DATA off	Hardware flow control			1	byte
t6	CTS-high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		µs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte

Figure 5-2 shows the UART data frame. Table 5-2 describes the symbols used in Figure 5-2.

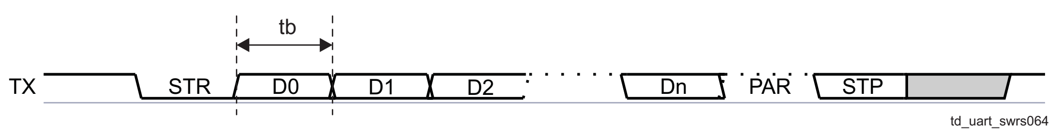


Figure 5-2. Data Frame

Table 5-2. Data Frame Key

Symbol	Description
STR	Start bit
D0...Dn	Data bits (LSB first)
PAR	Parity bit (optional)
STP	Stop bit

5.5.2 PCM

Figure 5-3 shows the interface timing for the PCM. Table 5-3 and Table 5-4 list the associated master and slave parameters, respectively.

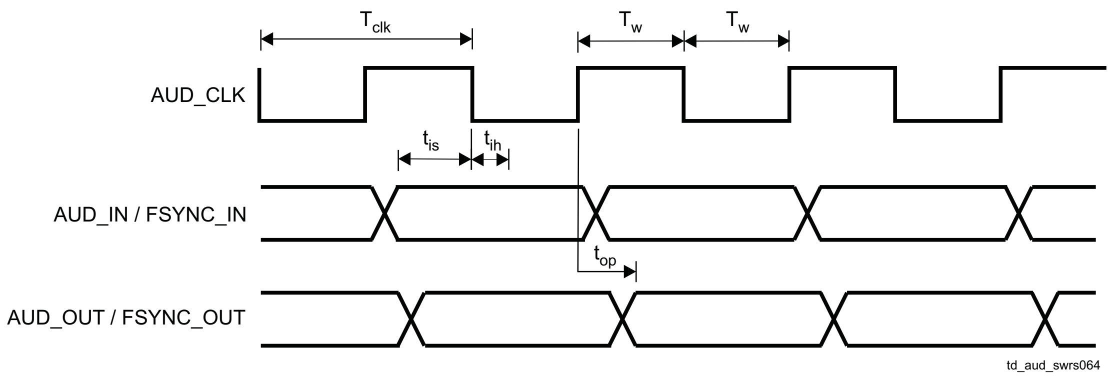


Figure 5-3. PCM Interface Timing

Table 5-3. PCM Master

Symbol	Parameter	Condition	Min	Max	Unit
T_{clk}	Cycle time		244.14 (4.096 MHz)	15625 (64 kHz)	ns
T_w	High or low pulse width		50% of T_{clk} min		
t_{is}	AUD_IN setup time		25		
t_{ih}	AUD_IN hold time		0		
t_{op}	AUD_OUT propagation time	40-pF load	0	10	
t_{op}	FSYNC_OUT propagation time	40-pF load	0	10	

Table 5-4. PCM Slave

Symbol	Parameter	Condition	Min	Max	Unit
T_{clk}	Cycle time		66.67 (15 MHz)		ns
T_w	High or low pulse width		40% of T_{clk}		
T_{is}	AUD_IN setup time		8		
T_{ih}	AUD_IN hold time		0		
t_{is}	AUD_FSYNC setup time		8		
t_{ih}	AUD_FSYNC hold time		0		
t_{op}	AUD_OUT propagation time	40-pF load	0	21	

PRODUCT PREVIEW

6 Reference Design for Power and Radio Connections

Figure 6-1 shows the reference schematics for the TI *Bluetooth* HCI module. Consult TI for complete schematics and PCB layout guidelines.

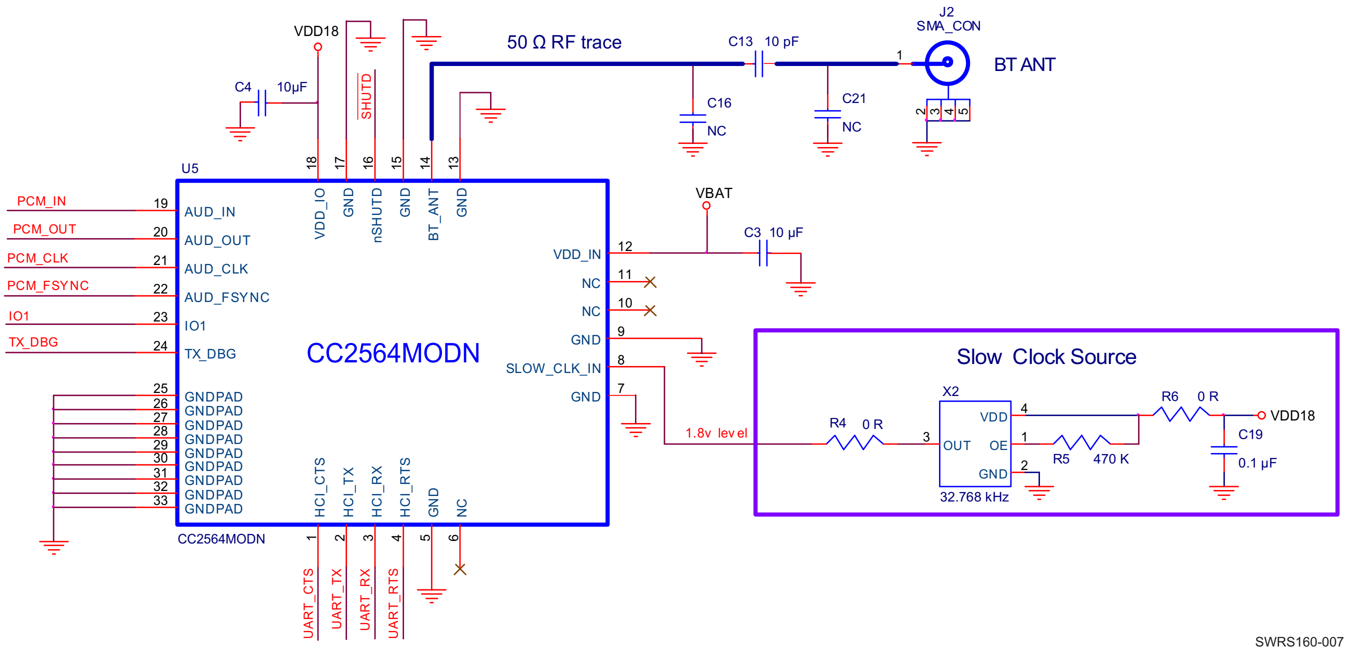


Figure 6-1. Reference Schematics

PRODUCT PREVIEW

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

For a complete listing of development-support tools, visit the Texas Instruments CC256x wiki. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.2 Device Support Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.

X Experimental, preproduction, sample or prototype device. Device may not meet all product qualification conditions and may not fully comply with TI specifications. Experimental/Prototype devices are shipped against the following disclaimer: “This product is still in development and is intended for internal evaluation purposes.” Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

null Device is qualified and released to production. TI’s standard warranty applies to production devices.

7.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.3 Trademarks

MSP430, DRP are trademarks of Texas Instruments.
Cortex, ARM7TDMIE are registered trademarks of ARM Limited.
ARM is a registered trademark of ARM Physical IP, Inc.
iPod is a registered trademark of Apple, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

PRODUCT PREVIEW

8 Mechanical, Packaging, and Orderable Information

8.1 Module Outline

Figure 8-1 shows the outline of the TI *Bluetooth* HCI module.

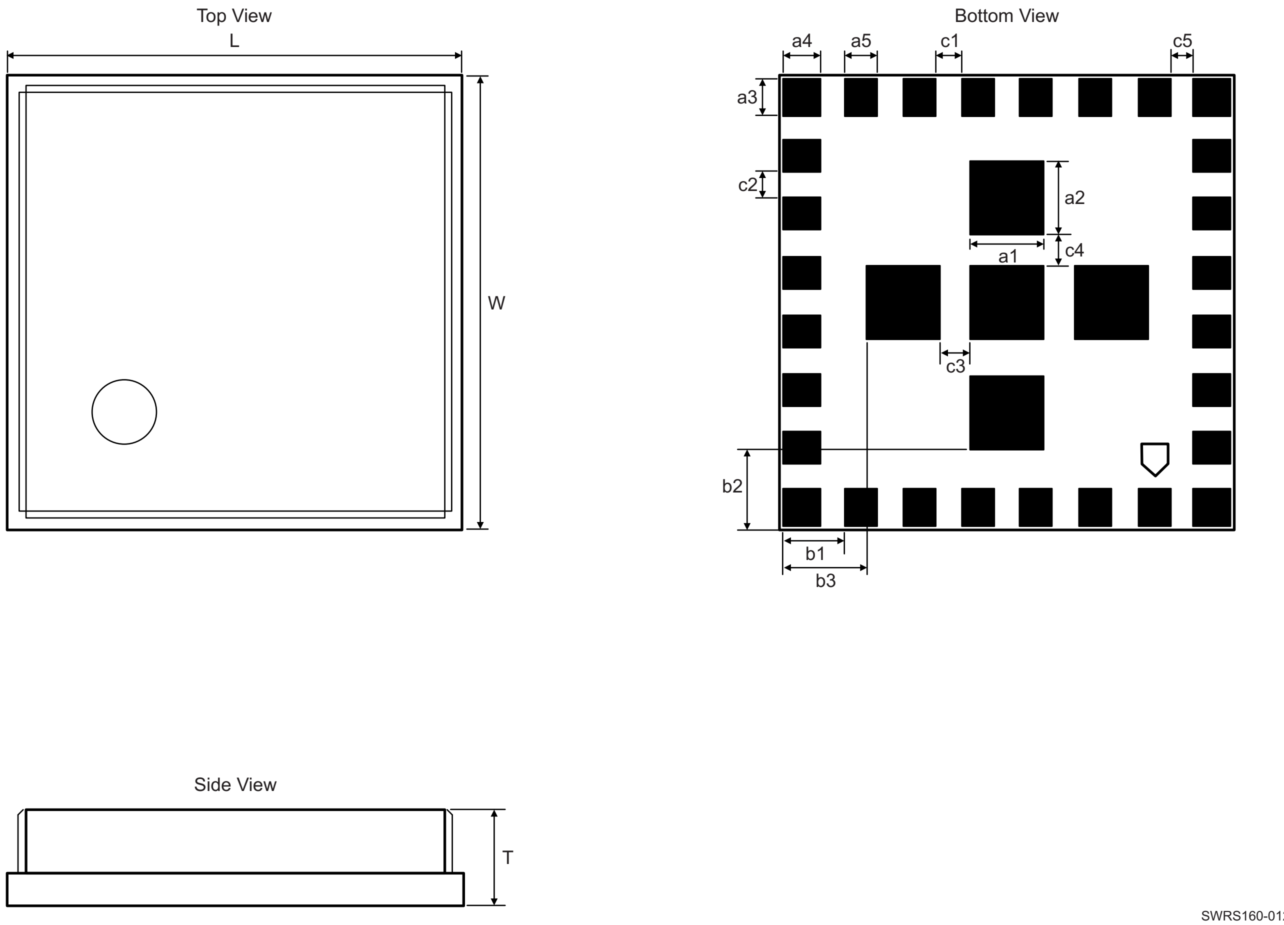


Figure 8-1. Outline of TI *Bluetooth* HCI Module

Table 8-1 lists the dimensions of the TI *Bluetooth* HCI module outline.

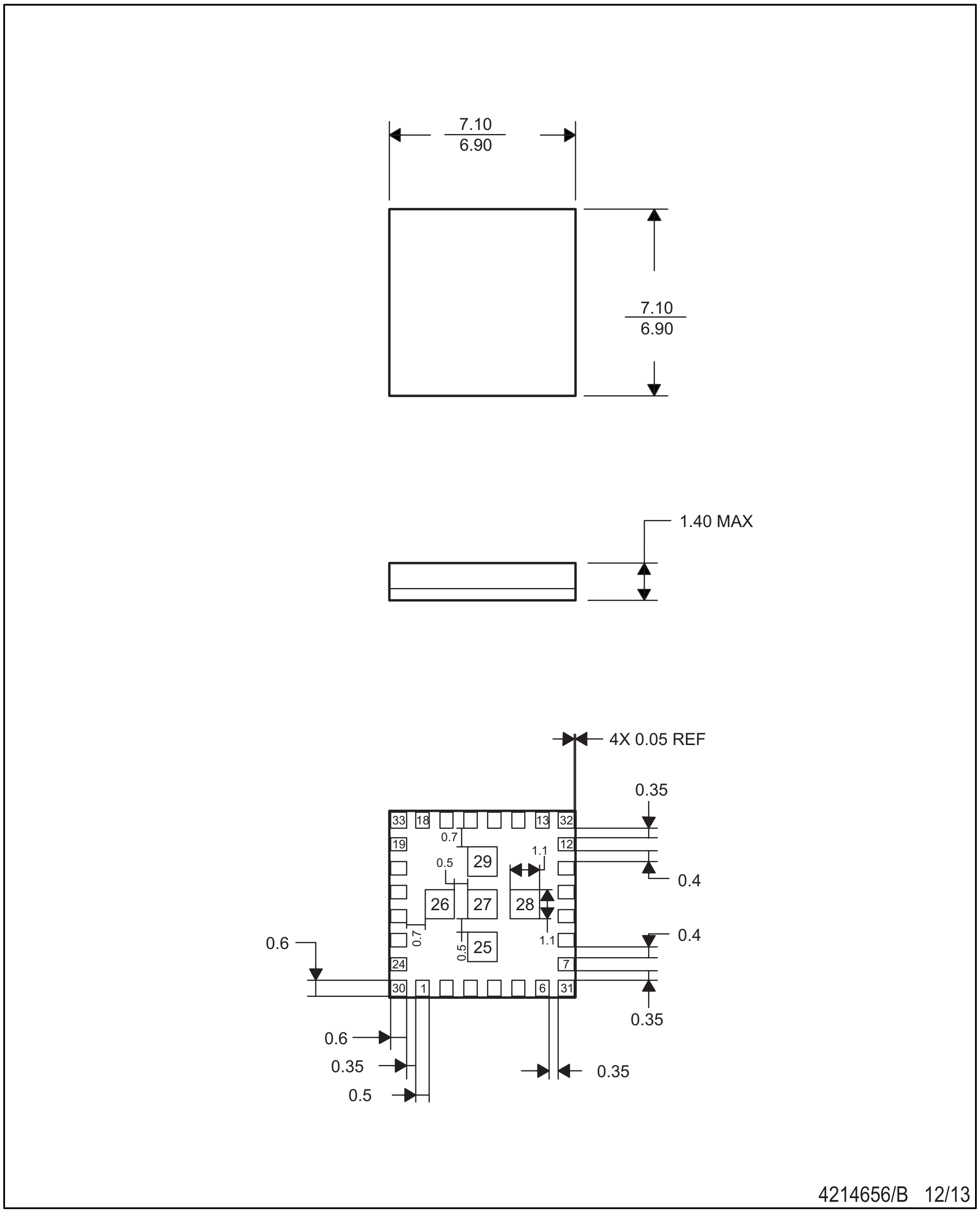
Table 8-1. Dimensions of TI *Bluetooth* HCI Module Mechanical Outline

Marking	Dimensions (mm)	Marking	Dimensions (mm)
L (body size)	7.0 (±0.1)	b1	0.95 (±0.1)
W (body size)	7.0 (±0.1)	b2	1.35 (±0.15)
T (thickness)	1.4 (max)	b3	1.35 (±0.15)
a1	1.1 (±0.15)	c1	0.4 (±0.05)
a2	1.1 (±0.15)	c2	0.4 (±0.05)
a3	0.6 (±0.1)	c3	0.5 (±0.1)
a4	0.6 (±0.1)	c4	0.5 (±0.1)
a5	0.5 (±0.1)	c5	0.35 (±0.05)

PRODUCT PREVIEW

8.2 Mechanical Data

MOE (S – MSIP – N33) METAL SINGLE–IN–LINE MODULE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.

SWRS160-019

PRODUCT PREVIEW

8.3 Chip Packaging and Ordering

8.3.1 Package and Ordering Information

Table 8-2. Package and Order Information

Part Number[(1)]	Status	Package Type	Minimum Orderable Quantity
XCC2564MODNCMOET	Preview	MOE	250
XCC2564MODNCMOER	Preview	MOE	2000

(1) Part number marking key:
- X – experimental (before qualification)
- CC2564 – module variant
- MODNC – module marking (commercial)
- MOEx – module package designator (R: tape/reel; T: small reel)

For example, XCC2564MODNCMOET = experimental CC2564 module, revision C, small reel.

Figure 8-2 shows the chip markings for the TI *Bluetooth* HCI module.

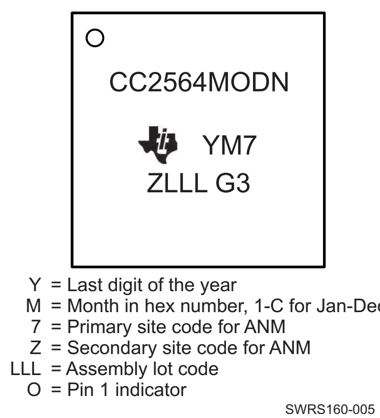


Figure 8-2. Chip Markings

8.3.2 Empty Tape Portion

Figure 8-3 shows the empty portion of the carrier tape.

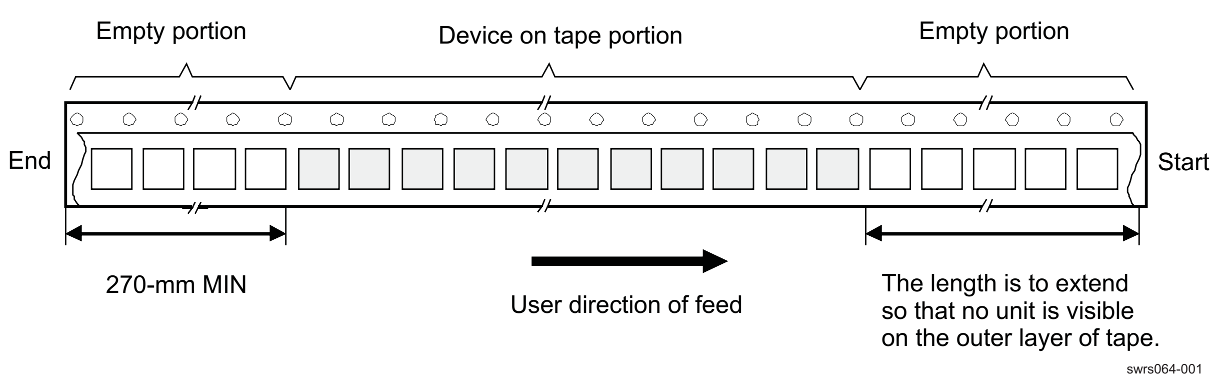


Figure 8-3. Carrier Tape and Pockets

8.3.3 Device Quantity and Direction

When pulling out the tape, the A1 corner is on the left side (see Figure 8-4).

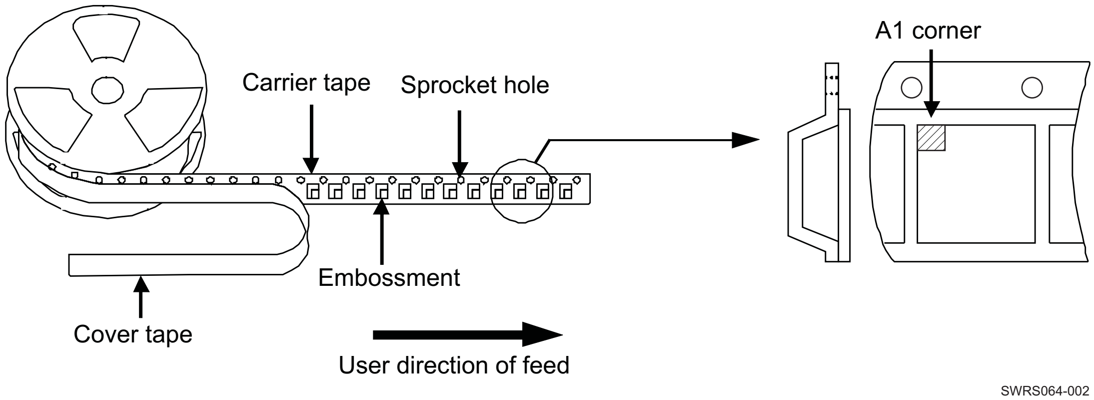


Figure 8-4. Direction of Device

8.3.4 Insertion of Device

Figure 8-5 shows the insertion of the device.

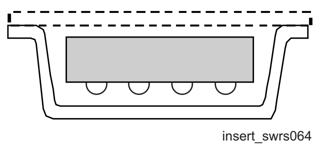


Figure 8-5. Insertion of Device

8.3.5 Tape Specification

Figure 8-6 shows the dimensions of the tape.

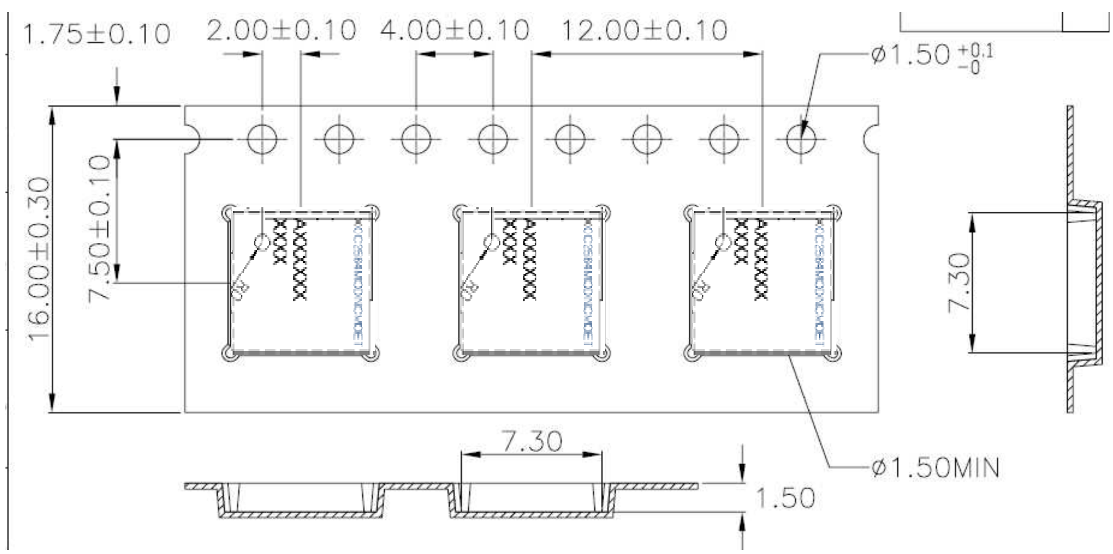


Figure 8-6. Tape Dimensions (mm)

- Cumulative tolerance of the 10-sprocket hole pitch is ±0.20.
- Carrier camber is within 1 mm in 250 mm.
- Material is black conductive polystyrene alloy.

PRODUCT PREVIEW

- All dimensions meet EIA-481-D requirements.
- Thickness: 0.30 ±0.05 mm
- Packing length per 22-inch reel is 110.5 m (1:3).
- Component load per 13-inch reel is 2000 pieces.

8.3.6 Reel Specification

Figure 8-7 shows the reel specifications:

- 330-mm reel, 12-mm width tape
- Reel material: Polystyrene (static dissipative/antistatic)

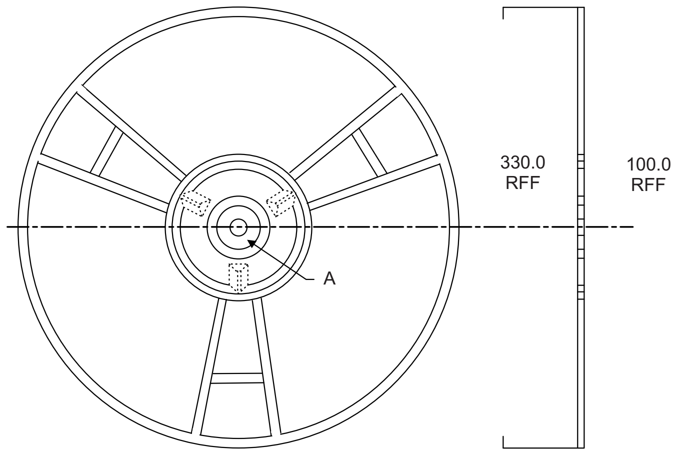


Figure 8-7. Reel Dimensions (mm)

8.3.7 Packing Method

Figure 8-8 shows the reel packing method.

PRODUCT PREVIEW

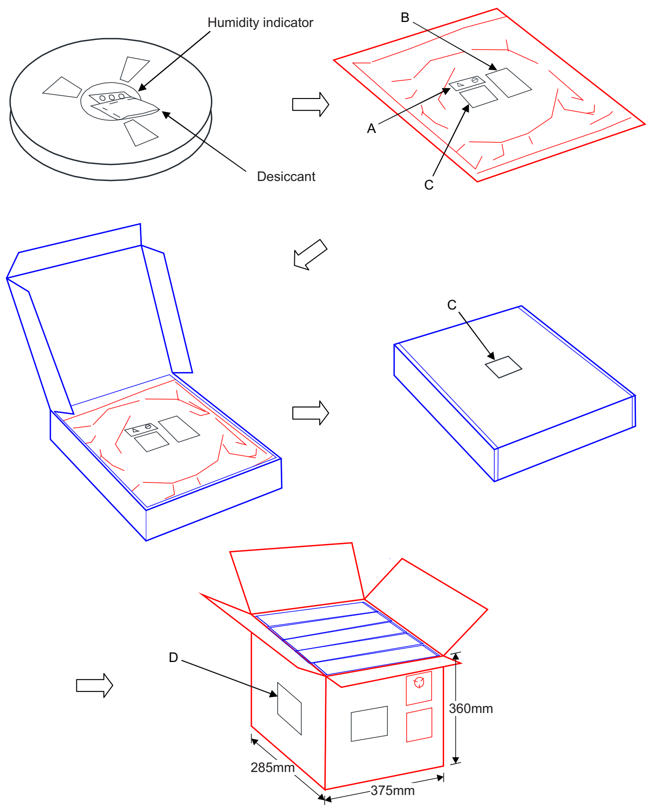


Figure 8-8. Reel Packing Method

8.3.8 *Packing Specification*

8.3.8.1 Reel Box

Each moisture-barrier bag is packed into a reel box, as shown in Figure 8-9.

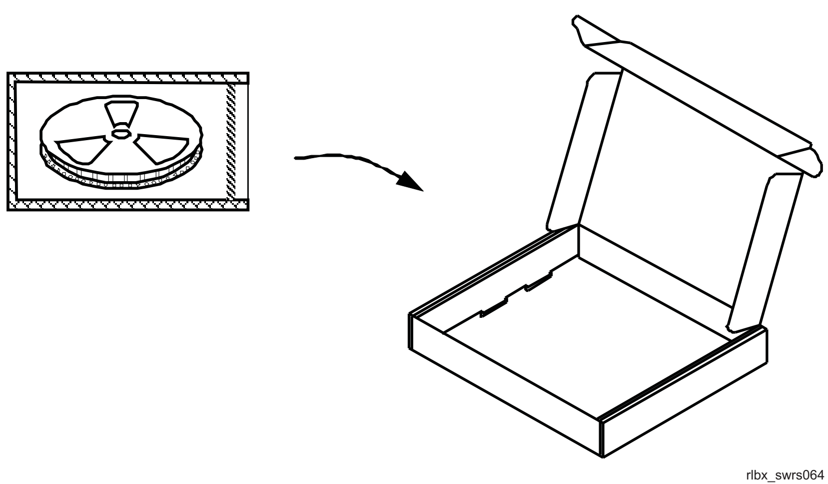


Figure 8-9. Reel Box (Carton)

8.3.8.2 Reel Box Material

The reel box is made from corrugated fiberboard.

PRODUCT PREVIEW

8.3.8.3 Shipping Box

If the shipping box has excess space, filler (such as cushion) is added.

Figure 8-10 shows a typical shipping box.

NOTE

The size of the shipping box may vary depending on the number of reel boxes packed.

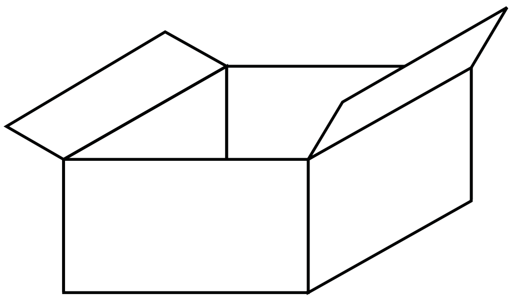


Figure 8-10. Shipping Box (Carton)

8.3.8.4 Shipping Box Material

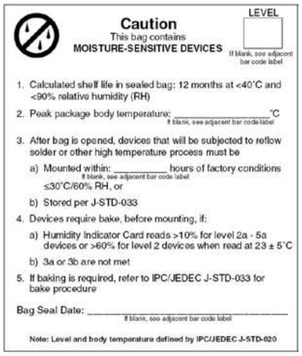
The shipping box is made from corrugated fiberboard.

8.3.8.5 Labels

Figure 8-11 shows the antistatic and humidity notice.

Figure 8-11. Antistatic and Humidity Notice

Figure 8-12 shows the MSL caution and storage condition notice.



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
If blank, see adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
2. Peak package body temperature: ____________ °C
   If blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: ________ hours of factory conditions
      If blank, see adjacent bar code label
      ≤30°C/60% RH, or
   b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C
   b) 3a or 3b are not met
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: ____________
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

Figure 8-12. MSL Caution and Storage Condition Notice

Figure 8-13 shows the label for the inner box.

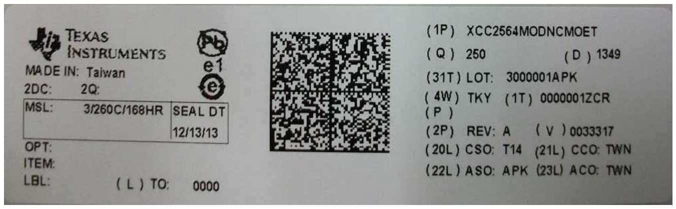


Figure 8-13. Label for the Inner Box

PRODUCT PREVIEW

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265