

XIO3130 Implementation Guide

Computer Connectivity Solutions

ABSTRACT

This document is provided to assist platform designers using the XIO3130 PCI Express (PCIe) Switch. Detailed information can be found in the [XIO3130 Data Manual](#). However, this document provides board design suggestions for the various device features when designing in the XIO3130.

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1 Typical System Implementation

Figure 1 shows a typical implementation of the XIO3130 PCI Express Switch. The device serves as a fanout switch between an upstream PCI Express device and up to 3 downstream PCI Express devices. The XIO3130 operates has a x1 upstream PCI Express interface as the primary bus and the three x1 downstream PCI Express interfaces as secondary busses. PCI Express reference clocks for the three downstream devices are provided by the XIO3130. These three reference clocks are frequency locked to the PCI Express reference clock input associated with the upstream port.

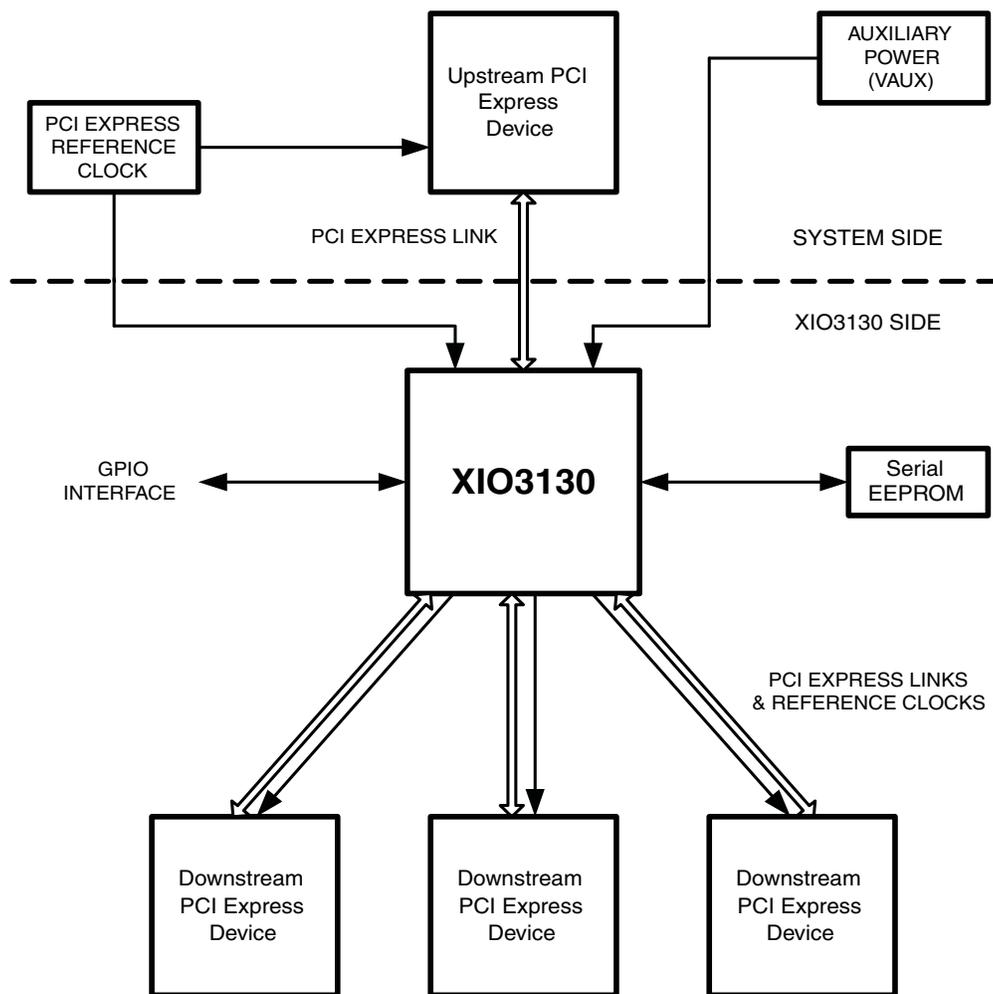


Figure 1. Typical System Implementation

A common differential 100-MHz PCI Express reference clock is required. Figure 1 illustrates the typical implementation.

If $V_{AUX33REF}$ power states are a system requirement, the XIO3130 fully supports this feature by maintaining system configuration information in “sticky” register bits.

An optional external EEPROM can be implemented to load various configuration registers but is not necessary if those registers are enumerated via software/BIOS for the system.

Up to nineteen general-purpose inputs and/or outputs (GPIOs) exist for further system customization. If PCI Hot Plug is required, GPIO options exist to fully support this feature and will require several GPIO pins per port that PCI Hot Plug is enabled.

2 Power Considerations

2.1 1.5-V and 3.3-V Digital Supplies

The XIO3130 requires both 1.5-V and 3.3-V digital power.

The 1.5-V terminals are named $V_{DD_{15}}$. These terminals supply power to the digital core. The 1.5-V core allows for a significant reduction in both power consumption and logic switching noise.

The 3.3-V terminals are named $V_{DD_{33}}$ and supply power to most of the input and output cells.

Both the $V_{DD_{15}}$ and $V_{DD_{33}}$ supplies must have 0.1- μ F bypass capacitors to V_{SS} (ground) in order for proper operation. The recommendation is one capacitor for each power terminal.

2.2 1.5-V and 3.3-V Analog Supplies

Both 1.5-V and 3.3-V analog power is required by the XIO3130. Since circuit noise on the analog power terminals must be minimized, filters are recommended. Until the XIO3130 is fully characterized, the following filters are recommended:

- $V_{DDA15(0)}$ – filter with three 0.1- μ F bypass capacitors and one 1000-pF bypass capacitor connected to V_{SS} (ground)
- $V_{DDA15(1)}$ – filter with three 0.1- μ F bypass capacitors and one 1000-pF bypass capacitor connected to V_{SS} (ground)
- $V_{DDA15(2)}$ – filter with three 0.1- μ F bypass capacitors and one 1000-pF bypass capacitor connected to V_{SS} (ground)
- $V_{DDA15(3)}$ – filter with three 0.1- μ F bypass capacitors and one 1000-pF bypass capacitor connected to V_{SS} (ground)
- V_{DDA33} – filter with one 0.1- μ F bypass capacitor connected to V_{SS} (ground)
- $V_{DD15REF}$ – filter with one 0.1- μ F bypass capacitor connected to V_{SS} (ground)
- $V_{DD33REF}$ – filter with one 0.1- μ F bypass capacitor connected to V_{SS} (ground)
- $V_{AUX33REF}$ – filter with one 0.1- μ F bypass capacitor connected to V_{SS} (ground)

High-speed board design rules must be followed when connecting bypass capacitors to V_{DDA} and V_{SS} .

2.3 Combined Power Outputs

To support $V_{AUX33REF}$ system requirements, the XIO3130 internally combines main power with $V_{AUX33REF}$ power. There are three combined power rails in the XIO3130. These three power rails are distributed to the analog circuits, digital logic, and I/O cells that must operate during the $V_{AUX33REF}$ state. Each of the three power rails has an output terminal for the external attachment of bypass capacitors to minimize circuit switching noise. These terminals are named $V_{DDCOMB_{15}}$, $V_{DDCOMB_{33}}$, and $V_{DDCOMB_{IO}}$.

The recommended bypass capacitors for each combined output terminal are 1000 pF, 0.01 μ F, and 1.0 μ F. When placing these capacitors on the bottom side of the circuit board, the smallest capacitor is positioned next to the via associated with the combined output terminal and the largest capacitor is the most distant from the via. The circuit board trace width connecting the combined output terminal via to the capacitors must be at least 12 to 15 mils wide with the trace length as short as possible.

Other than the three recommended capacitors, no external components or devices may be attached to these combined output terminals.

2.4 Auxiliary Power

If V_{AUX} power is available in the system, the XIO3130 has the $V_{AUX33REF}$ terminal to support this feature. Without fully understanding a system's V_{aux} power distribution design, recommending external components for the XIO3130 is difficult. At a minimum, a 0.1- μ F bypass capacitor is placed near the XIO3130 and attached to the system's $V_{AUX33REF}$ power supply. A robust design may include a filter with bulk capacitors (5 μ F to 100 μ F) to minimize voltage fluctuations. When the system is cycling main power or is in the $V_{AUX33REF}$ state, the $V_{AUX33REF}$ terminal requirements are that the input voltage cannot exceed 3.6 V or drop below 3.0 V for proper operation of the switch.

If V_{AUX} power is not present within the system, this terminal is connected to V_{SS} through 1 k Ω resistor and the \overline{WAKE} terminal should not be connected to the system in order to prevent a possible \overline{WAKE} assertion at power-up before the part has been properly reset..

2.5 V_{SS} and V_{SSA} Terminals

For proper operation of the XIO3130, a unified V_{SS} and V_{SSA} ground plane is recommended. The circuit board stack-up recommendation is to implement a layer two ground plane directly under the XIO3130 device.

2.6 Capacitor Selection Recommendations

When selecting bypass capacitors for the XIO3130 device, a low ESR capacitor such as the X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and cost of these capacitors make them a logical choice for most computer systems

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low-frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell "D" size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce low-frequency power supply noise and ripple.

2.7 Power-Up/Down Sequencing

All XIO3130 analog and digital power terminals must be controlled during the power-up and power-down sequence. Absolute maximum power terminal ratings must not be exceeded to prevent damaging the device. All power terminals must remain within 3.6 V to prevent damaging the XIO3130.

When sequencing the 1.5-V and 3.3-V power terminals, they may be sequenced in any order with any time relationship and with any ramp rate. For additional power sequencing requirements, please reference the *XIO3130 Data Manual* (literature number [SCPS212](#)) and the *PCI-Express Card Electromechanical Specification*, Revision 2.0.

2.8 Power Supply Filtering Recommendations

To meet the PCI-Express jitter specifications, low-noise power is required on several of the XIO3130 voltage terminals. The power terminals that require low-noise power include VDDA15(0), VDDA15(1), VDDA15(2), VDDA15(3), VDDA33, VDD15REF, VDD33REF, and VAUX33REF. This section provides guidelines for the filter design to create low-noise power sources.

The least expensive solution for low-noise power sources is to filter existing 3.3 V and 1.5 V power supplies. This solution requires analysis of the switching noise present on the power supplies. The XIO3130 has external interfaces operating at clock rates of 100 MHz, and 1.25 GHz. Other devices located near the XIO3130 may produce switching noise at different frequencies. Also, the power supplies that generate the 3.3 V and 1.5 V power rails may add low frequency ripple noise. Linear regulators have feedback loops that typically operate in the 100 kHz range. Switching power supplies typically have operating frequencies in the 500 KHz range. When analyzing power supply noise frequencies, the first, third, and fifth harmonic of every clock source should be considered.

Critical analog circuits within the XIO3130 must be shielded from this switching noise. The fundamental requirement for a filter design is to reduce switching noise to a peak-to-peak amplitude of less than 25 millivolts. This maximum noise amplitude should apply to all frequencies from 0 Hz to 6.25 GHz.

The following information should be considered when designing a power supply filter:

- Ideally, the series resonance frequency for each filter component should be greater than the fifth harmonic of the maximum clock frequency. With a maximum clock frequency of 1.25 GHz, the third harmonic is 3.75 GHz and the fifth harmonic is 6.25 GHz. Finding inductors and capacitors with a series resonance frequency above 6.25 GHz is both difficult and expensive. Components with a series resonance frequency in the 4 to 6 GHz range are a good compromise.
- The inductor(s) associated with the filter must have a DC resistance low enough to pass the required current for the connected power terminals. The voltage drop across the inductor must be low enough

to meet the minus 10% voltage margin requirement associated with each XIO3130 power terminal. Power supply output voltage variation must be considered as well as voltage drops associated with any connector pins and circuit board power distribution geometries.

- The Q versus frequency curve associated with the inductor must be appropriate to reduce power terminal noise to less than the maximum peak-to-peak amplitude requirement for the XIO3130. Recommending a specific inductor is difficult because every system design is different and therefore the noise frequencies and noise amplitudes are different. Many factors will influence the inductor selection for the filter design. Power supplies must have adequate input and output filtering. A sufficient number of bulk and bypass capacitors are required to minimize switching noise. Assuming that board level power is properly filtered and minimal low frequency noise is present, frequencies less than 10 MHz, an inductor with a Q greater than 20 from approximately 10 MHz to 3 GHz should be adequate for most system applications.
- The series component(s) in the filter may either be an inductor or a ferrite bead. Testing has been performed on both component types. When measuring PCI-Express link jitter, the inductor or ferrite bead solutions produce equal results. When measuring circuit board EMI, the ferrite bead is a superior solution.

NOTE: The XIO3130 reference schematics include ferrite beads in the analog power supply filters.

- When designing filters associated with power distribution, the power supply is a low impedance source and the device power terminals are a low impedance load. The best filter for this application is a T filter. See [Figure 2](#) for a T-filter circuit. Some system may require this type of filter design if the power supplies or nearby components are exceptionally noisy. This type of filter design is recommended if a significant amount of low frequency noise, frequencies less than 10 MHz, is present in a system.
- For most applications a Pi filter will be adequate. See [Figure 2](#) for a Pi-filter circuit. When implementing a Pi filter, the two capacitors and the inductor must be located next to each other on the circuit board and must be connected together with wide low impedance traces. Capacitor ground connections must be short and low impedance.
- If a significant amount of high frequency noise, frequencies greater than 300 MHz, is present in a system, creating an internal circuit board capacitor will help reduce this noise. This is accomplished by locating power and ground planes next to each other in the circuit board stackup. A gap of 0.003 mils between the power and ground planes will significantly reduce this high frequency noise.
- Another option for filtering high-frequency logic noise is to create an internal board capacitor using signal layer copper plates. When a component requires a low-noise power supply, usually the Pi filter is located near the component. Directly under the Pi filter, a plate capacitor may be created. In the circuit board stack-up, select a signal layer that is physically located next to a ground plane. Then, generate an internal 0.25 inch by 0.25 inch plate on that signal layer. Assuming a 0.006 mil gap between the signal layer plate and the internal ground plane, this will generate a 12 pF capacitor. By connecting this plate capacitor to the trace between the Pi filter and the component's power terminals, an internal circuit board high frequency bypass capacitor is created. This solution is extremely effective for switching frequencies above 300 MHz.

[Figure 2](#) illustrates two different filter designs that may be used with the XIO3130 to provide lownoise power to critical power terminals.

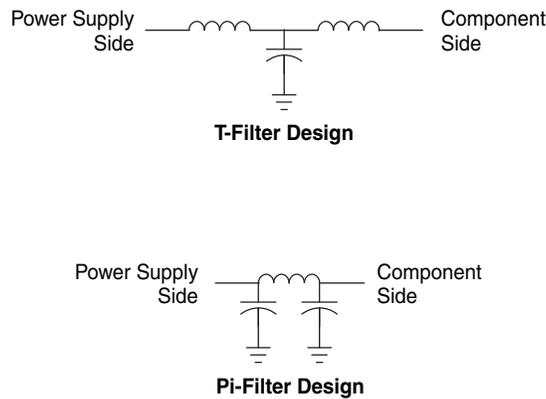


Figure 2. Filter Designs

3 PCI Express Interface Considerations

The XIO3130 has an x1 PCI Express interface that runs at 2.5 Gb/s and is fully compliant to the *PCI Express Base Specification*, Revision 2.0. The remainder of this section describes implementation considerations for the XIO3130 primary and secondary PCI Express interfaces.

3.1 Upstream 2.5-Gb/s Transmit and Receive Links

The XIO3130 upstream port attaches to an upstream PCI Express device over a 2.5-Gb/s high-speed differential transmit and receive PCI Express x1 link. The connection details are provided in [Table 1](#).

Table 1. XIO3130/PCI Express Device Terminal Connection Details

TERMINAL NAME		COMMENTS
XIO3130	UPSTREAM PCI EXPRESS DEVICE	
UP_PETp (G1)	RXP	XIO3130's transmit positive differential terminal connects to the upstream device's receive positive differential terminal.
UP_PETn (G2)	RXN	XIO3130's transmit negative differential terminal connects to the upstream device's receive negative differential terminal.
UP_PERp (J1)	TXP	XIO3130's receive positive differential terminal connects to the upstream device's transmit positive differential terminal.
UP_PERn (J2)	TXN	XIO3130's receive negative differential terminal connects to the upstream device's transmit negative differential terminal.

3.2 Downstream 2.5-Gb/s Transmit and Receive Links

The XIO3130 upstream port attaches to an upstream PCI Express device over a 2.5-Gb/s high-speed differential transmit and receive PCI Express x1 link. The connection details are provided in [Table 2](#).

Table 2. XIO3130/PCI Express Device Terminal Connection Details

TERMINAL NAME		COMMENTS
XIO3130	UPSTREAM PCI EXPRESS DEVICE	
DN1_PETp (A8)	RXP Device 1	XIO3130 Port 1 transmit positive differential terminal connects to the downstream device receive positive differential terminal.
DN1_PET (B8)	RXN Device 1	XIO3130 Port 1 transmit negative differential terminal connects to the downstream device receive negative differential terminal.
DN1_PERp (A6)	TXP Device 1	XIO3130 Port 1 receive positive differential terminal connects to the downstream device transmit positive differential terminal.

Table 2. XIO3130/PCI Express Device Terminal Connection Details (continued)

TERMINAL NAME		COMMENTS
XIO3130	UPSTREAM PCI EXPRESS DEVICE	
DN1_PERn (B6)	TXN Device 1	XIO3130 Port 1 receive negative differential terminal connects to the downstream device transmit negative differential terminal.
DN2_PETp (H13)	RXP Device 2	XIO3130 Port 2 transmit positive differential terminal connects to the downstream device receive positive differential terminal.
DN2_PETn (H14)	RXN Device 2	XIO3130 Port 2 transmit negative differential terminal connects to the downstream device receive negative differential terminal.
DN2_PERp (F13)	TXP Device 2	XIO3130 Port 2 receive positive differential terminal connects to the downstream device transmit positive differential terminal.
DN2_PERn (F14)	TXN Device 2	XIO3130 Port 2 receive negative differential terminal connects to the downstream device transmit negative differential terminal.
DN3_PETp (N7)	RXP Device 3	XIO3130 Port 3 transmit positive differential terminal connects to the downstream device receive positive differential terminal.
DN3_PETn (P7)	RXN Device 3	XIO3130 Port 3 transmit negative differential terminal connects to the downstream device receive negative differential terminal.
DN3_PERp (N9)	TXP Device 3	XIO3130 Port 3 receive positive differential terminal connects to the downstream device transmit positive differential terminal.
DN3_PERn (P9)	TXN Device 3	XIO3130 Port 3 receive negative differential terminal connects to the downstream device transmit negative differential terminal.

3.3 PCI Express Link Routing Guidelines

The XIO3130 TXP and TXN terminals comprise a low-voltage, 100- Ω differentially driven signal pair. The RXP and RXN terminals for the XIO3130 receive a low-voltage, 100- Ω differentially driven signal pair. The XIO3130 has integrated 50- Ω termination resistors to V_{SS} on both the RXP and RXN terminals eliminating the need for external components.

Each lane of the differential signal pair must be ac-coupled. The recommended value for the series capacitor is 0.1 μ F. To minimize stray capacitance associated with the series capacitor circuit board solder pads, 0402-sized capacitors are recommended.

When routing a 2.5-Gb/s low-voltage, 100- Ω differentially driven signal pair, the following circuit board design guidelines must be considered:

1. The PCI-Express drivers and receivers are designed to operate with adequate bit error rate margins over a 20" maximum length signal pair routed through FR4 circuit board material.
2. Each differential signal pair must be 100- Ω differential impedance with each single-ended lane measuring in the range of 50 Ω to 55 Ω impedance to ground.
3. The differential signal trace lengths associated with a PCI Express high-speed link must be length matched to minimize signal jitter. This length matching requirement applies only to the P and N signals within a differential pair. The transmitter differential pair does not need to be length matched to the receiver differential pair. The absolute maximum trace length difference between the TXP signal and TXN signal must be less than 5 mils. This also applies to the RXP and RXN signal pair.
4. If a differential signal pair is broken into segments by vias, series capacitors, or connectors, the length of the positive signal trace must be length matched to the negative signal trace for each segment. Trace length differences over all segments are additive and must be less than 5 mils.
5. The location of the series capacitors is critical. For add-in cards, the series capacitors are located between the TXP/TXN terminals and the PCI-Express connector. In addition, the capacitors are placed near the PCI Express connector. This translates to two capacitors on the motherboard for the downstream link and two capacitors on the add-in card for the upstream link. If both the upstream device and the downstream device reside on the same circuit board, the capacitors are located near the TXP/TXN terminals for each link.
6. The number of vias must be minimized. Each signal trace via reduces the maximum trace length by approximately 2 inches. For example: if 6 vias are needed, the maximum trace length is 8 inches.

7. When routing a differential signal pair, 45 degree angles are preferred over 90 degree angles. Signal trace length matching is easier with 45-degree angles and overall signal trace length is reduced.
8. The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.
9. If vias are used to change from one signal layer to another signal layer, it is important to maintain the same 50- Ω impedance reference to the ground plane. Changing reference planes causes signal trace impedance mismatches. If changing reference planes cannot be prevented, bypass capacitors connecting the two reference planes next to the signal trace vias will help reduce the impedance mismatch.
10. If possible, the differential signal pairs must be routed on the top and bottom layers of a circuit board. Signal propagation speeds are faster on external signal layers.

3.4 PCI Express Transmitter Reference Resistor

The REFR0 (D2) and REFR1 (E3) terminals connect to an external resistor to set the drive current for the PCI Express TX driver. The recommended resistor value is 14,532 Ω with 1% tolerance.

A 14,532- Ω resistor is a custom value. To eliminate the need for a custom resistor, two series resistors are recommended: a 14,300- Ω , 1% resistor and a 232- Ω , 1% resistor. Trace lengths must be kept short to minimize noise coupling into the reference resistor terminals.

3.5 PCI Express Reference Clock Inputs

The XIO3130 requires an external reference clock for the PCI-Express interface. The *PCI Express Base Specification* and *PCI Express Card Electromechanical Specification* provide information concerning the requirements for this reference clock. The XIO3130 is designed to meet all stated specifications when the reference clock input is within all PCI Express operating parameters. This includes both standard clock oscillator sources or spread spectrum clock oscillator sources.

The XIO3130 requires a 100-MHz differential reference clock. A single clock source with multiple differential clock outputs is connected to all PCI Express devices in the system. The differential connection between the clock source and each PCI Express device is point-to-point. This system implementation is referred to as a common clock design.

The UP_REFCKIp (L1) and UP_REFCKIn (L2) terminals provide differential reference clock inputs to the XIO3130. The circuit board routing rules associated with the 100-MHz differential reference clock are the same as the 2.5-Gb/s transmit and receive link routing rules itemized in [Section 3.3](#). The only difference is that the differential reference clock does not require series capacitors. The requirement is a DC connection from the clock driver output to the XIO3130 receiver input. Electrical specifications for these differential inputs are included in the *XIO3130 Data Manual*.

Terminating the differential clock signal is circuit board design specific. But, the XIO3130 design has no internal 50- Ω -to-ground termination resistors. Both REFCKI inputs, at approximately 20 k Ω to ground, are high-impedance inputs.

3.6 PCI Express Reference Clock Outputs

The XIO3130 contains a PCI Express reference clock fanout circuit. The REFCKI differential receiver drives three differential output drivers, one differential output driver for each downstream device. The naming convention for one of the reference clock output drivers is DNx_REFCKOp and DNx_REFCKOn, where x is the downstream port number 1, 2, or 3. The package terminal output differential pairs are M11/M12, P13/P14, and N12/N13. The reference clock outputs require both a 20 series resistance and 50 termination to ground (see [Figure 3](#).)

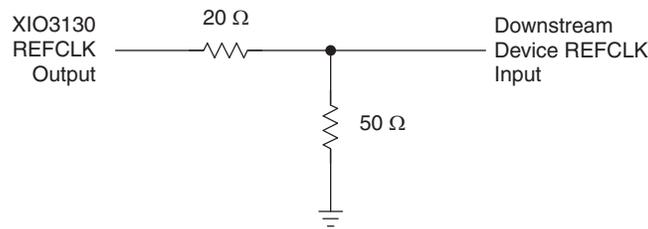


Figure 3. Reference Clock Output

3.7 PCI Express Reset

The XIO3130 receives a PCI Express reset from the upstream device on the UP_ $\overline{\text{PERST}}$ terminal (B1). The XIO3130 provides a PCI Express reset individually to each downstream device on the DNx_ $\overline{\text{PERST}}$ terminals. The B1 input cell has hysteresis and is operational during both the main power state and V_{AUX33REF} power state. No external components are required.

Please reference the *XIO3130 Data Manual* and *PCI-Express Card Electromechanical Specification* to fully understand the $\overline{\text{PERST}}\#$ electrical requirements and timing requirements associated with power-up and power-down sequencing. Also, the *XIO3130 Data Manual* identifies all configuration and memory-mapped register bits that are reset by $\overline{\text{PERST}}$.

3.8 PCI Express Wake

With regards to implementing either $\overline{\text{WAKE}}$ or Beacon to re-activate the PCI Express link hierarchy's main power rails and reference clocks, the XIO3130 supports the following three options:

1. If the $\overline{\text{WAKE}}$ option is selected, $\overline{\text{WAKE}}$ is an open-drain output from the XIO3130 that is driven low when a Beacon signal is received on any one of the three downstream port's DN_PER terminals during the L2 state.
2. If the Beacon option is selected, a Beacon signal is generated on the upstream port's UP_PET terminals when a Beacon signal is received on any of the three downstream port's DN_PER terminals during the L2 state.
3. If the $\overline{\text{WAKE}}$ to Beacon option is selected, the $\overline{\text{WAKE}}$ terminal is an input that when driven low will cause the Upstream Port's UP_PET terminals to generate a Beacon signal during the L2 state.

Bits 2:1 of the upstream port's Global Chip Control register at offset 0B8h must be programmed to enable option 1 or option 3. Option 2 is the power-on default.

When $\overline{\text{WAKE}}$ is an open-drain output, a system side pullup resistor is required to prevent the signal from floating. The drive capability of this open-drain output is 4 mA. Therefore, the value of the selected pullup resistor must be large enough to assure a logic low signal level at the receiver. A robust system design will select a pullup resistor value that de-rates the output driver current capability by a minimum of 50%. At 3.3 V with a de-rated drive current equal to 2 mA, the minimum resistor value is 1.65 k Ω . Larger resistor values are recommended to reduce the current drain on the V_{AUX33REF} supply.

When $\overline{\text{WAKE}}$ to Beacon is enabled, $\overline{\text{WAKE}}$ is an input requiring a pull-up resistor to V_{AUX33REF} (if supported) or V_{DD33} (if V_{AUX33REF} is not supported) to prevent the signal from floating. The drive strength for each PCI Express downstream device that is connected to the XIO3130 $\overline{\text{WAKE}}$ input must be researched to determine the minimum value for the pullup resistor. Larger resistor values are recommended to reduce the current drain on the V_{AUX33REF} supply.

4 Miscellaneous Terminal Considerations

4.1 GPIO Terminals

There are 19 general purpose input/output (GPIO) terminals in the XIO3130. All GPIO terminals are 3.3 V inputs or outputs. The power-up default for the GPIO terminals is input mode with an internal active pull-up to 3.3 V.

The DN_x_DSPTRP (where x = port #, 1, 2, or 3) if pulled-high at the de-assertion of reset will cause some of the GPIO terminals to be mapped to PCI Hot Plug terminals for the various ports. If DN1_DPSTRP is pulled high, then GPIO0, GPIO1, and GPIO2 will be mapped to PCI Hot Plug terminals for downstream port 0. If DN2_DPSTRP is pulled high, then GPIO4, GPIO5, and GPIO6 will be mapped to PCI Hot Plug terminals for downstream port 2. If DN3_DPSTRP is pulled high, then GPIO8, GPIO9, and GPIO10 will be mapped to PCI Hot Plug terminals for downstream port 3. GPIOs that are mapped to hot plug functions by these strapping options will not be available for other uses and will ignore their respective settings in the GPIO control registers.

For the remaining GPIO bits, there are configuration register bits in the upstream port's proprietary register space that control and/or monitor these terminals. The GPIO A, B, C, and D register bits at offset 0BCh and 0C0h allow for individual GPIO bit control. Control options include either input mode, output mode, or the function described in the register bit description. The GPIO DATA register bits at offset 0C4h are used to monitor GPIO terminals in input mode and are used to set the logic state of GPIO terminals in output mode.

4.2 \overline{GRST} Terminal

\overline{GRST} is a global reset terminal that is provided for custom reset requirements. When this input is asserted low, all registers, state machines, digital logic, and analog circuits are returned to their power-up default state. This reset is asynchronous to the external PCI Express reference clock and all internal clock domains. The \overline{GRST} input buffer has hysteresis. This input is powered either by main power or by $V_{AUX33REF}$ power. Therefore, global resets may be initiated during either power state.

During an XIO3130 device power-up from the D3 cold power state, there is no requirement to assert this terminal low. An internal power-up reset function performs an equivalent reset to \overline{GRST} . Since this input is powered during $V_{AUX33REF}$ states, it is imperative that any external circuits connected to \overline{GRST} do not erroneously drive this input low when main power is lost. This results in the reset of sticky control bits and power management state machines.

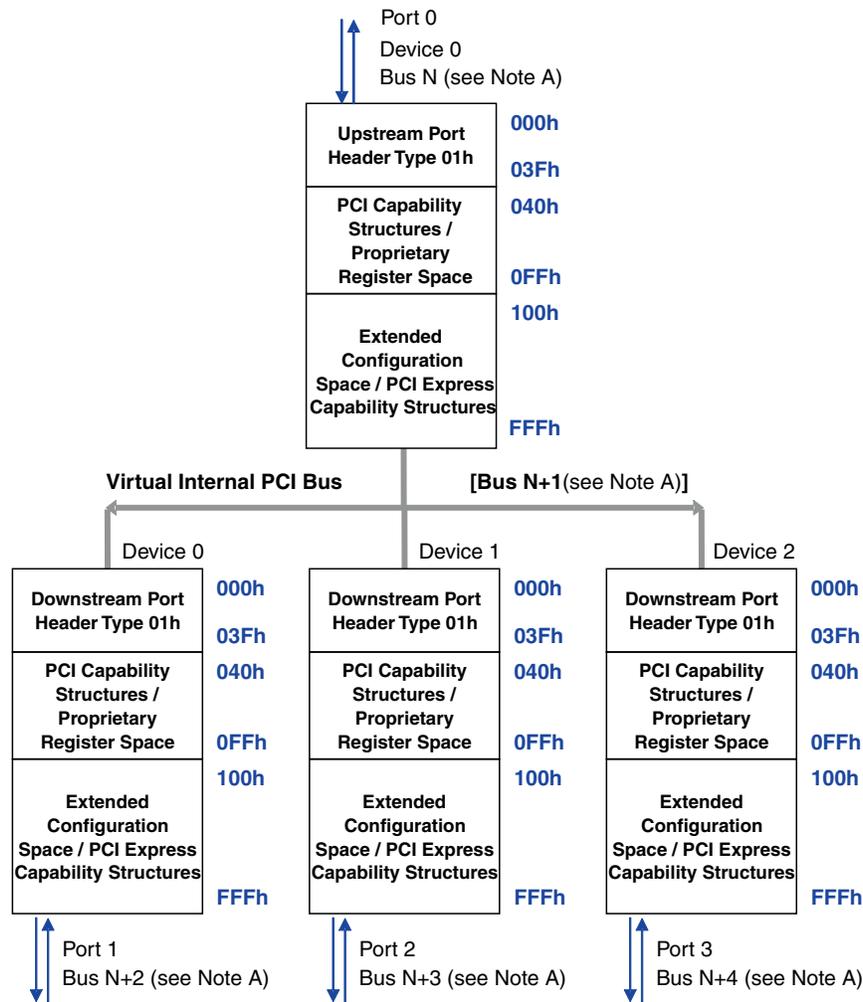
A pullup resistor tied to $V_{AUX33REF}$ (if supported) or 3.3V (if $V_{AUX33REF}$ is not supported) is required to keep this terminal high unless this terminal is driven by an upstream device. If this terminal is driven, by an upstream device, the pull-up resistor may only be removed if this terminal is driven de-asserted as well as asserted (i.e. it may not be removed if connected to an open-drain source).

4.3 Reserved Terminals

The XIO3130 has five reserved input terminals. These terminals have requirements to be pulled to 1.5 V, pulled to 3.3 V, or pulled to ground. The requirements for the specific terminals are listed in the *XIO3130 Data Manual*. These terminals must be terminated to the proper levels to ensure correct operation of the XIO3130.

5 Software Considerations

The XIO3130 PCI Express Switch is natively supported by either BIOS software and/or operating system software that recognizes the classic PCI-to-PCI bridge programming model. The XIO3130 will appear to host software logically as 3 PCI to PCI bridges directly behind a PCI to PCI bridge (see figure 3). XIO3130 classic PCI configuration register space uses a type 1 PCI bridge header. All other XIO3130 advanced features will default to a disabled state and do not require configuration register initialization for basic operation. However, to fully utilize advanced features within the XIO3130, custom device drivers will be required.



A Example values, actual bus numbers may change based on system hierarchy

Figure 4. XIO3130 Logical Topology

5.1 Serial EEPROM Interface Configuration

An external serial EEPROM port is provided on the XIO3130 for power-up configuration support. Typically, the system BIOS initializes the configuration registers associated with the serial EEPROM feature. But for custom systems or PCI-Express add-in cards, this feature is provided to automate basic XIO3130 configuration register initialization.

The registers loaded by the serial EEPROM feature are located in the PCI configuration space. The names of these registers include the subsystem ID and subsystem vendor ID, GPIO control registers, and General Control.

NOTE: The serial EEPROM also loads TI proprietary registers. The data loaded into these bytes must not be changed from the values specified in the EEPROM register loading map. Otherwise, the operational state of the XIO3130 is indeterminate.

Terminal B14 named SCL, provides a basic EEPROM enable or disable option. When $\overline{\text{PERST}}$ is deasserted, the logic state of this terminal is checked. If a 1b is detected, the serial EEPROM interface is enabled. A 0b disables the interface. An external pullup or pulldown resistor is required to generate the appropriate logic state.

Immediately after the detection of a 1b on terminal L08, the XIO3130 performs the following actions:

1. Bit 3 (SBDETECT) in the serial-bus control and status register is set.
2. Bit 4 (ROMBUSY) in the serial-bus control and status register is set and a serial EEPROM download is initiated to device address 1010_000Xb and word address 00h.
3. The EEPROM will serially load values from the EEPROM and place values in registers indicated in the EEPROM Loading map.
4. When the serial EEPROM interface state machine is finished, the ROMBUSY status bit is deasserted. If any errors are detected during the download procedure, bit 0 (ROM_ERR) in the serial-bus control and status register is set. If ROM_ERR status is asserted, the state of any configuration register targeted by the EEPROM download is unknown.

Additional detail is provided in the *XIO3130 Data Manual* related to the serial EEPROM function and configuration register download map.

5.2 BIOS Considerations

This section provides a high-level overview of the registers which need to be programmed by the BIOS upon initialization of the XIO3130. Registers must be programmed to match the system implementation.

5.3 Classic PCI Configuration Registers

Primary Bus Number Register (PCI offset 18h)

This register indicates the bus number of the PCI bus segment that the primary PCI Express interface is connected to. The switch uses this information to determine how to respond to a type 0 configuration transaction. The register default is 00h.

Secondary Bus Number Register (PCI offset 19h)

This register indicates the bus number of the PCI bus segment that the secondary PCI interface is connected to. The bridge uses this information to determine how to respond to a type 1 configuration transaction. The register default is 00h.

Subordinate Bus Number Register (PCI offset 1Ah)

This register indicates the bus number of the highest number PCI bus segment that is downstream of the bridge. The bridge uses this information to determine how to respond to a type 1 configuration transaction. The register default is 00h.

Subsystem Vendor ID and Subsystem ID Registers (PCI offsets 84h and 86h)

These registers are used for subsystem and option card identification purposes. Typically, these registers contain the OEM vendor ID and an OEM identified designator. These fields can be programmed using the EEPROM or BIOS. If using BIOS, the subsystem access register at offset E0h is written to update the subsystem vendor ID and subsystem ID registers.

GPIO Control and Data Registers (PCI offsets BCh, BEh, C0h, C2h, and C4h)

These registers determine the function of the GPIO terminals and set the default state for all GPIO outputs. The initialization state for these registers is system architecture dependent. The control register default is GPIO input mode. GPIO terminals that are strapped to hotplug functions by using the DNx_DPSTRP pins will not be affected by values written into these registers.

General Control Register (PCI offset D4h)

This register controls various bridge power management and interface operation specific functions that are fully described in the *XIO3130 Data Manual*. This register can be programmed using the EEPROM or BIOS.

Memory Base and Limit Registers (PCI offsets 20h through 2Ch)

These registers determine the region of memory, prefetchable and non-prefetchable, that is available to devices behind each bridge. Since the XIO3130 is composed of 4 “virtual” bridges, each bridge will have a region of memory that can be assigned to devices downstream of that bridge. The upstream port’s memory region must encompass the memory region of all the downstream ports as all devices downstream of the XIO3130 are downstream of the upstream port, each downstream port will have a memory region that is exclusive of the other downstream ports as a given address can not be on two

different busses. The base address registers set the lower limit for the addresses that will be forwarded while the limit registers determine the upper limit. If a memory transaction is received on the upstream port with an address that falls between a window's base and limit registers, it will be forwarded to the secondary side of the bridge; if the limit is lower than the base then the window is invalid and will not be used in the memory decode.

I/O Base and Limit Registers (PCI offsets 1Ch, 1Dh, 30h, and 32h)

These registers are identical to the Memory Base and Limit Registers described above but are used to determine the addresses of I/O transactions that will be forwarded beyond the virtual bridges of the XIO3130.

6 Power Management Considerations

6.1 D3/L2 Power Management Information

The *PCI Express Card Electromechanical Specification* contains a section that specifies the operation of a PCI Express device when transitioning from D0/L0 to D3/L2 and back to D0/L0 power management states. Since the primary interface on the XIO3130 is PCI Express, the bridge supports this specification for both D3_{hot} and D3_{cold} power management states. System software has the option to place the bridge into the D3/L2 power management state. This process is started in the bridge by setting the PWR_STATE field in the power management control and status register to 11b. By following the procedure outlined in the *PCI Express Card Electromechanical Specification*, the bridge may be transitioned to either the D3_{hot} or D3_{cold} states to reduce system power.

The XIO3130 may initiate the power management state transition from D3/L2 back to D0/L0 either by asserting the WAKE signal or by issuing a BEACON on the upstream port, which mechanism is used is determined by bit 10 (WAKE_OR_BCN) in the global chip control register at offset B8h in PCI.

Downstream devices may also initiate the power management state transition from D3/L2 back to D0/L0 either by asserting the WAKE signal or by issuing a BEACON. If a downstream device asserts the WAKE signal, the XIO3130 can be enabled to transmit a BEACON on its upstream port which may serve to enable cabled applications, to enable this functionality the XIO3130 must be set to use BEACON as its wake event mechanism and bit 1 (WAKE2BCN) of the global chip control register must be set. If the XIO3130 receives a BEACON from a downstream device and is using BEACON as its wake event mechanism, it will transmit BEACON on its upstream port to alert the upstream device of the event. If the XIO3130 is asserting WAKE or signaling BEACON, it will continue to do so until power is restored as indicated by the deassertion of PERST.

A V_{AUX33REF} power terminal, coupled with internal circuits that combine main power and V_{AUX33REF} power, supplies power to the logic that controls power management state transitions from D3_{cold} back to D0/L0. Internal "sticky" logic maintains not only the content of specific switch PCI register bits, but also information about the operational states of the switch including state machine context and other internal mechanisms. PERST has no effect on the internal "sticky" logic.

6.2 Active-State Power Management Information

The PCI Express interface on the XIO3130 has the ability to automatically reduce power when there is no queued bus activity. Once this feature is enabled by software, the XIO3130 device automatically transitions into and out of a low power state. The switch supports both the L0's and L1 active state power management (ASPM) requirements.

In the PCI Express link capabilities registers, two 3-bit exit latency fields specify the latency time required for the link to transition from either the L0's or L1 state back to the L0 state. In the PCI Express device capabilities register, two 3-bit acceptable latency fields specify the maximum latency time that the switch will tolerate for the attached upstream PCI Express device to transition from either the L0's or L1 state back to the L0 state. The acceptable latency fields are an indirect measure of the switch's internal buffering.

Power management software uses the reported acceptable latency number to compare against the exit latencies reported by all components physically located on the PCI-Express link between the switch and the Root Complex to determine whether ASPM entry can be used with no significant impact to system performance.

ASPM must be individually enabled or disabled for each of the 4 links.

6.3 Power Override Information

System software has the ability to manually reduce power on the downstream PCI Express ports using the switch's power override feature. During system initialization, XIO3130 configuration registers must be loaded with system specific power information and power override instructions. After this initial setup, the PCI Express set slot power limit message may be used to either enable or disable the power override feature.

During system initialization the following configuration register fields are loaded. These fields are loaded by either the BIOS or serial EEPROM.

- The general control register contains MIN_POWER_SCALE and MIN_POWER_VALUE fields that are loaded with the power information associated with the bridge and all downstream PCI bus devices.
- The general control register contains a POWER_OVRD field that is loaded with the secondary PCI bus power override option.
- If the power override option associated with disabling secondary clocks is selected, the clock mask register should be initialized.

After the previously described initialization procedure, the PCI Express set slot power limit message may be used to either enable or disable the power override feature. If the scale and value power information in the PCI Express message is less than the general control register SCALE and VALUE fields, then the power override feature is enabled. If the scale and value power information in the PCI Express message is equal to or greater than the SCALE and VALUE fields, then the power override feature is disabled.

7 Reference Documents

- *PCI Express Base Specification*, Revision 1.1
- *PCI Express Card Electromechanical Specification*, Revision 1.0a
- *Express Card Standard*, Release 1.2 10.
- *XIO3130 Data Manual*, literature number [SLLS693](#)
- *Hot Plug on the XIO3130*, literature number TBD
- *XIO3130 EVM User's Guide*, literature number [SLLU108](#)

Revision History

DATE	REVISION	COMMENTS
08/2009	–	Initial release
05/2012	A	Improved image quality of the schematics

8 Reference Schematics

The following schematics show a simple implementation of the XIO3130.

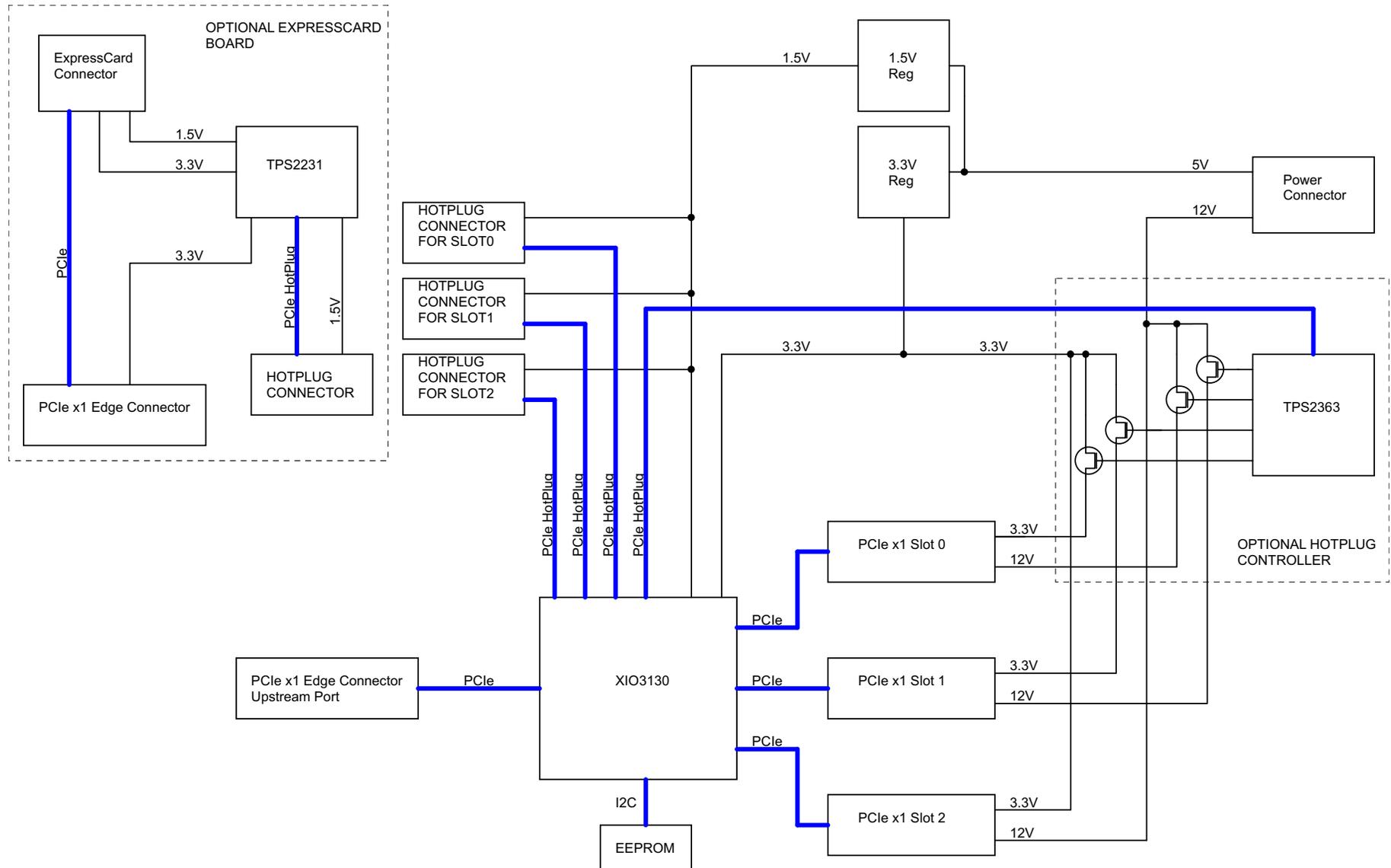


Figure 5. XIO3130 Schematic (Sheet 1 of 4)

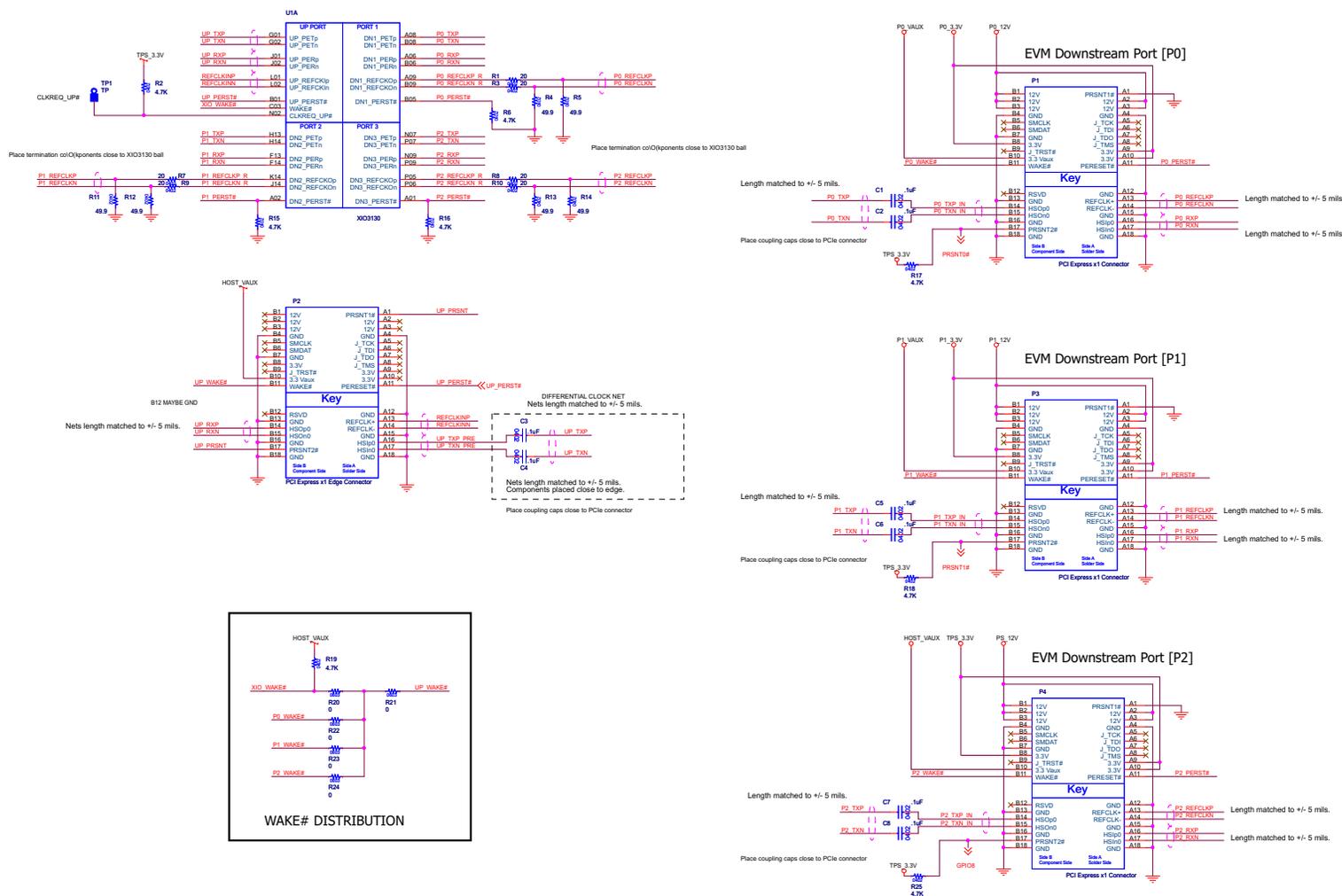


Figure 6. XIO3130 Schematic (Sheet 2 of 4)

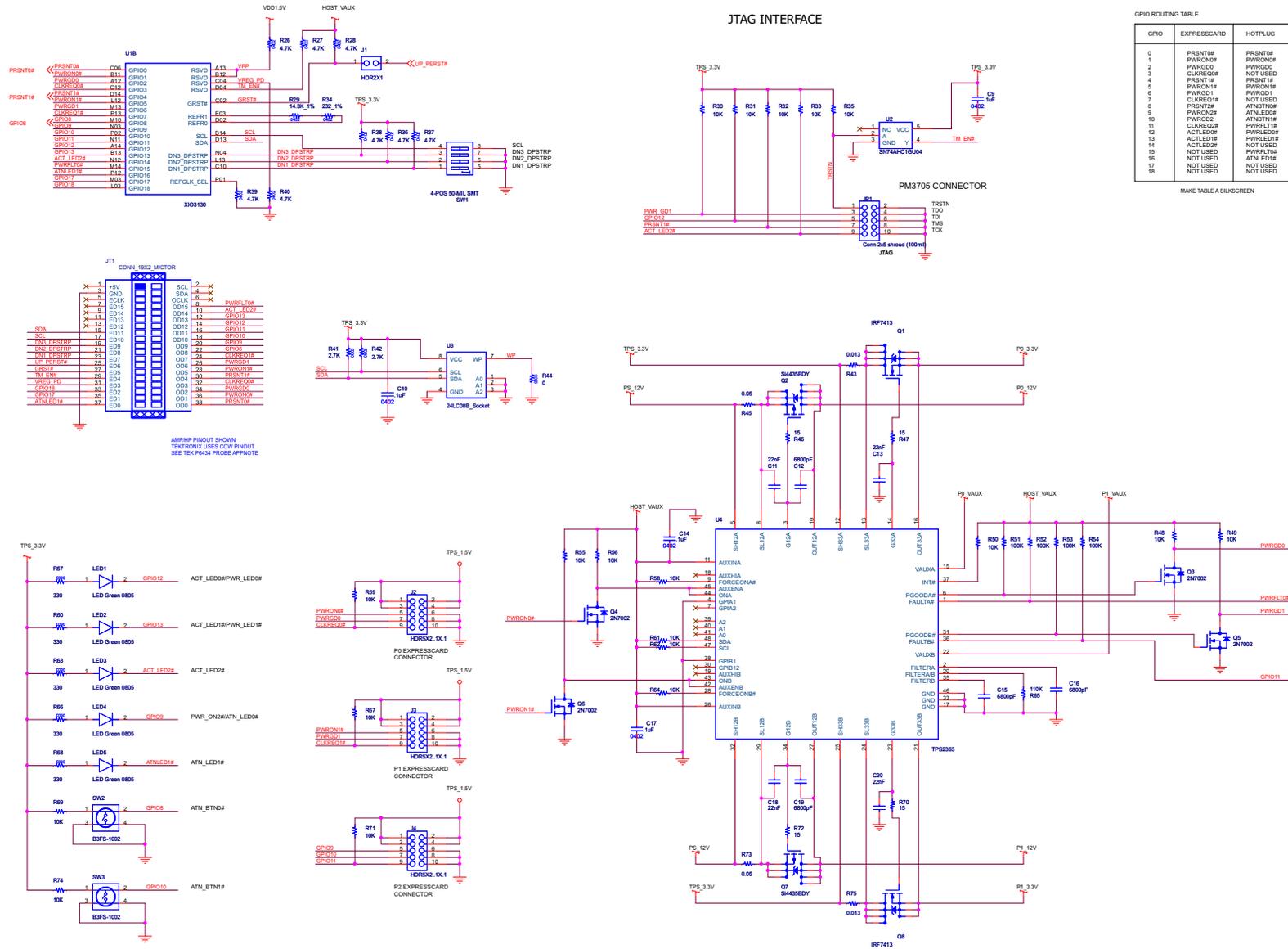


Figure 7. XIO3130 Schematic (Sheet 3 of 4)

POWER

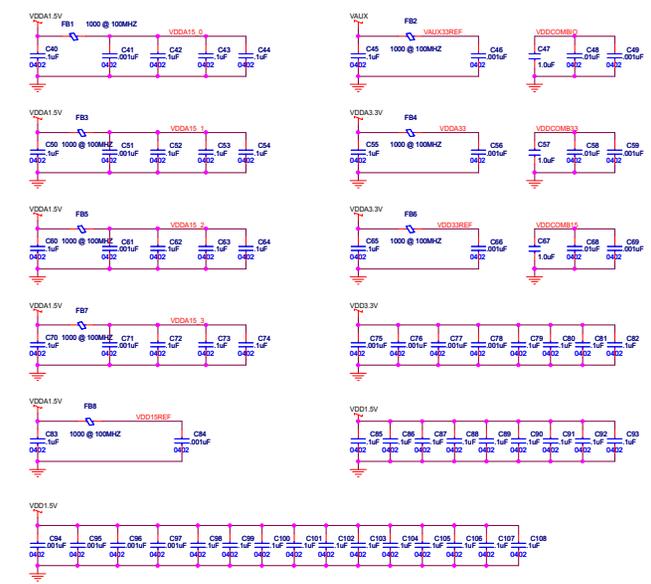
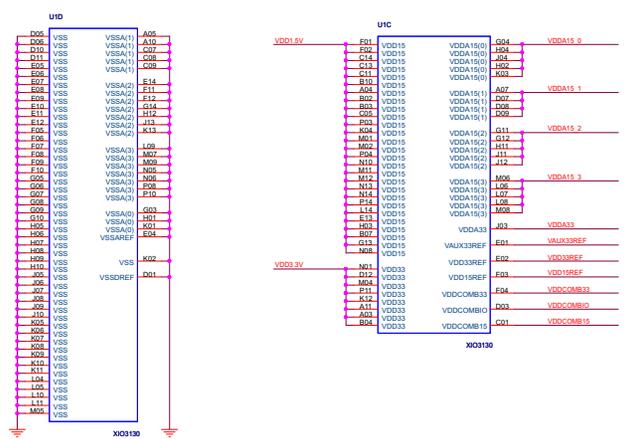
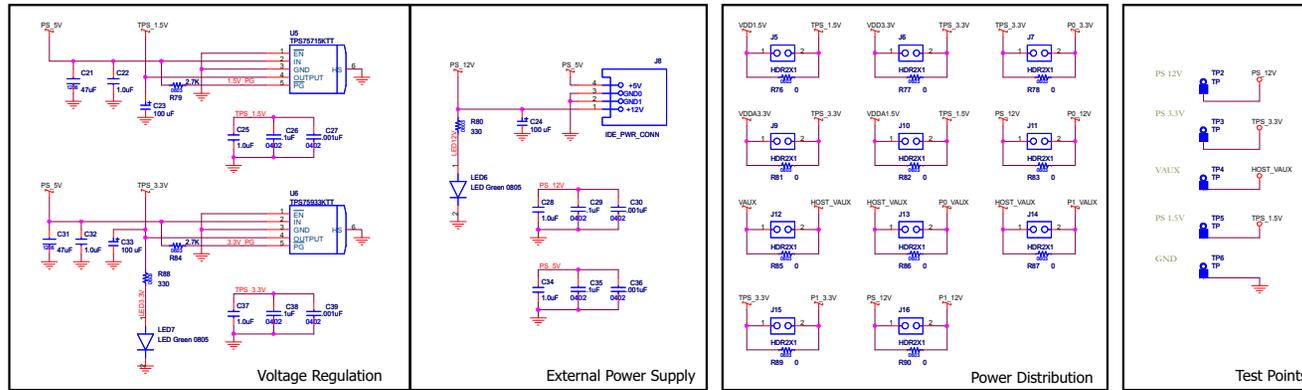


Figure 8. XIO3130 Schematic (Sheet 4 of 4)

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