

Reset Circuit for the TMS320C6000 DSP

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Abstract

This document describes two solutions used to provide a reset circuit to the Texas Instruments (TI™) TMS320C6000 digital signal processor (DSP). One solution sets a supply voltage supervisor, such as the TI TLC7733 and TLC7725, on each of the supply voltages, DVdd and CVdd. Another solution monitors both the 2.5-V/1.8-V and 3.3-V power supplies using a single supervisor such as the TI TPS3707. This allows the DSP to be released from reset only if both its power supplies are at the proper levels..

To ensure that the TMS320C6000 does not generate signals unless the supply voltages are at appropriate levels, it is necessary to place a supervisor on the power supplies. Whenever the device is powered up, it should be held in reset until both the 3.3-V I/O supply (DVdd) and the 2.5-V core supply (CVdd) reach nominal values. Likewise, the device should be held in reset anytime either supply falls below a certain threshold value (88%).

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Design Problem

How do I provide a reset circuit to the TMS320C6000?

Solution

To ensure that the TMS320C6000 does not generate signals unless the supply voltages are at appropriate levels, it is necessary to place a supervisor on the power supplies. Whenever the device is powered up, it should be held in reset until both the 3.3-V I/O supply (DVdd) and the 2.5-V core supply (CVdd) reach nominal values. Likewise, the device should be held in reset anytime either supply falls below a certain threshold value (88%).

One simple way to accomplish both of these tasks is to set a supervisor on each of the supply voltages, DVdd and CVdd. For example, the Texas Instruments TLC7733 and TLC7725 voltage supervisors each assert a /RESET signal (active low) during power-up when their supply voltage reaches 1 V. This signal continues to be asserted until DVdd reaches its threshold voltage (plus an additional delay period),¹ at which time the device is released from reset. The /RESET signal is reasserted anytime the voltage level falls below 90% (2.93 V for the TLC7733 and 2.25 V for the '7725).

In addition to holding the DSP in reset while not fully powered-up, the TLC77xx also allows an externally generated signal to generate the /RESET assertion. This signal could result from another device driving a reset signal or a manual pushbutton switch being depressed. If both a digital signal and a manual reset are used in the design, the two signals should be combined logically (AND gate), then connected to /RESIN of the first supervisor. All external reset signals should go through the supervisor circuit.² If an external reset is introduced after the supervisor circuit, the timing delay requirements may not be met.

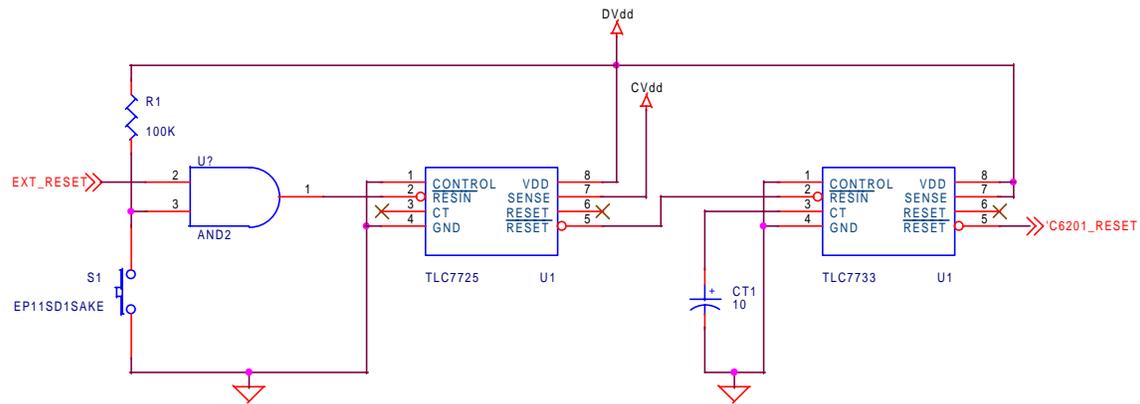
Figure 1 shows a sample circuit for the 'C6000 using the supervisor chip, which monitors both supply voltages and allows for both a manual (pushbutton) and externally generated reset. The second-stage supervisor should set the delay time to ensure that it is constant regardless of the cause of the reset.

¹ The delay period is determined by the capacitor CT of the reset circuit. In the design example provided, the delay times are <40 ns (see the TLC7733 and TLC7725 data sheet for propagation times with CT = NC) for the first stage and 210 ms for the second stage.

² All inputs to /RESIN must meet the minimum pulse requirement of 1 μ s, with rise and fall times of less than 10 ms.



Figure 1. Reset Circuit Using TLC77xx³



The delay time set by the reset circuit should be determined by considering the switch-on time of several components, which are summarized in Table 1.

Table 1. Setting Delay Timing t_d

	Switch-On Time (ms)
Line operated power supply	10–100
Battery power supply	0.03–30
Oscillator (start-up time)	10–100
Reset program	Several microseconds
Range of delay times t_d to be set	20–500

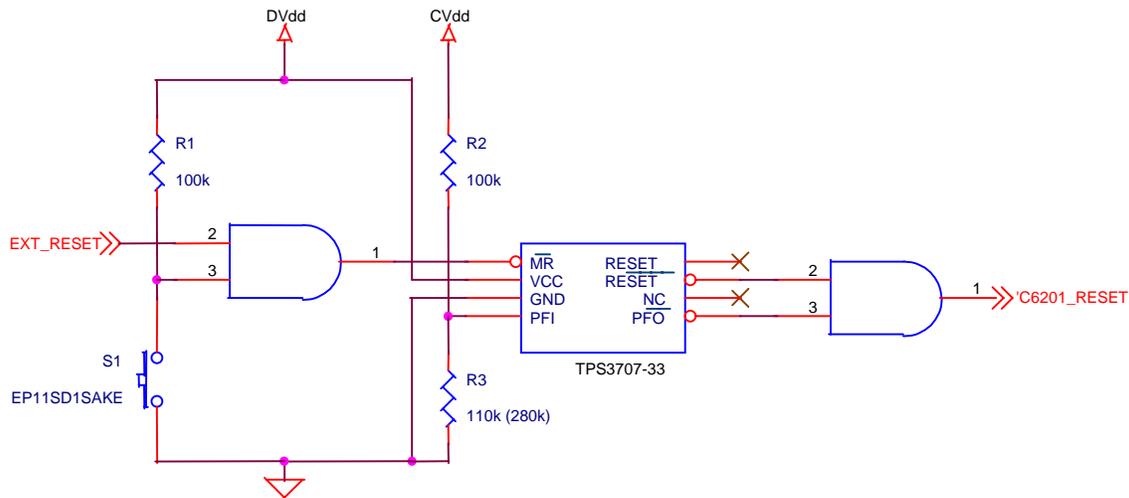
For additional information about designing with the TLC77xx supervisors, see the application report, *TLC77xx Series of BICMOS Supply Voltage Supervisors*.

Another solution is available using the TPS3707 to monitor both the 2.5-V/1.8-V and 3.3-V power supplies. This allows the DSP to be released from reset only if both its power supplies are at the proper levels. This can be easily done with a device that is also available in an 8-pin package and does not require an external capacitor to set its reset pulse width. It requires two resistors to set the 1.8/2.5 voltage selection.

Figure 2 shows a reference diagram showing the reset circuit using the TI TPS3707-33.

³ To provide a reset circuit that could be used for revision 3 and later, it would be necessary to use the TLC7701 (threshold voltage = 1.1 V) in place of the TLC7725 with a voltage divider to the SENSE input. Please see the TLC77xx data sheet for selecting voltage divider resistors.

Figure 2. Reset Circuit Using the TPS3707-33⁴



References

- Kohl, Ingrid. *TLC77xx Series of BiCMOS Supply Voltage Supervisors*, Literature number SLVAE03, April 1995, Texas Instruments.
- Haseloff, Eilhard. *Supply Voltage Supervisor TLC77xx Series*, Literature number SLVAE04, March 1997, Texas Instruments.
- TLC7701, TLC7725, TLC7703, TLC7733, TLC7705 Micropower Supply Voltage Supervisors Data Sheet*, Literature number SLVS087, March 1999, Texas Instruments.
- TPS3705-30, TPS3705-33, TPS3705-50, TPS3707-25, TPS3707-30, TPS3707-33, TPS3707-50 Processor Supervisory Circuits With Power-Fail Data Sheet*, Literature number SLVS184B, January 1999, Texas Instruments.
- Kornmeier, Bernd. *The TPS370x Family Application Report*, Literature number SLVA045, November 1998, Texas Instruments.

⁴ The circuit shown is for CVdd = 2.5 V. For CVdd = 1.8 V, use the resistor value in parentheses for R3.



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