MC74VHC257

Quad 2-Channel Multiplexer with 3-State Outputs

The MC74VHC257 is an advanced high speed CMOS quad 2−channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2−input digital multiplexers with common select (S) and enable ($\overline{OE}$) inputs. When ($\overline{OE}$) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: t_{PD} = 4.1 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: FETs = 100; Equivalent Gates = 25
- These Devices are Pb−Free and are RoHS Compliant

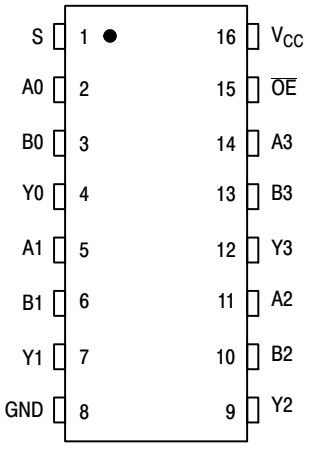

Figure 1. Pin Assignment

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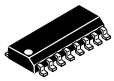
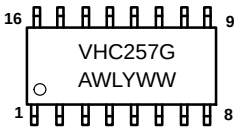
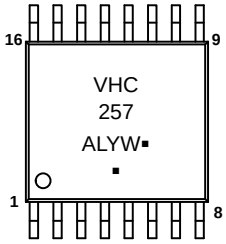
MARKING DIAGRAMS



SO−16
D SUFFIX
CASE 751B



TSSOP−16
DT SUFFIX
CASE 948F



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC257DG	SO−16	48 Units/Rail
MC74VHC257DR2G	SO−16	2500 Units/Reel
MC74VHC257DTG	TSSOP−16	96 Units/Rail
MC74VHC257DTR2G	TSSOP−16	2500 Units/Reel

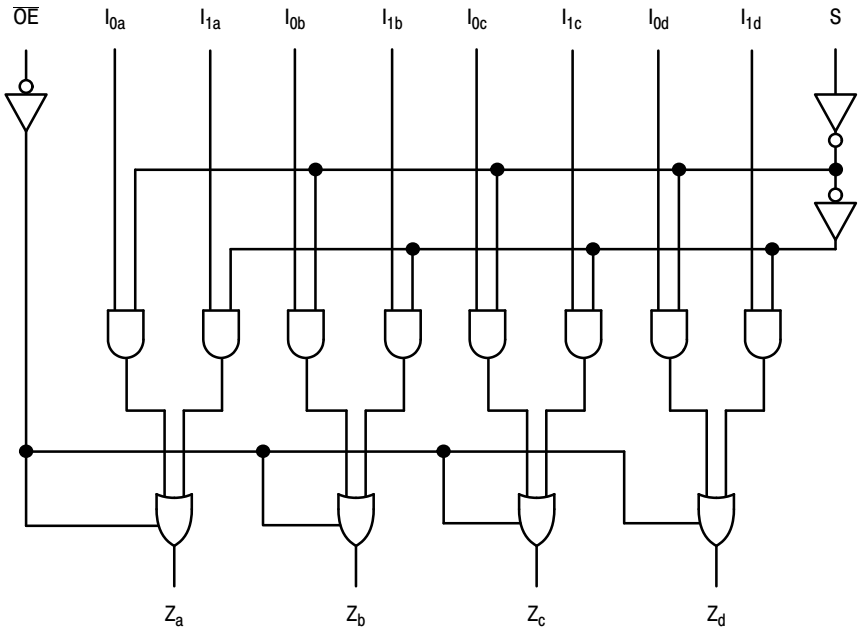


Figure 2. Expanded Logic Diagram

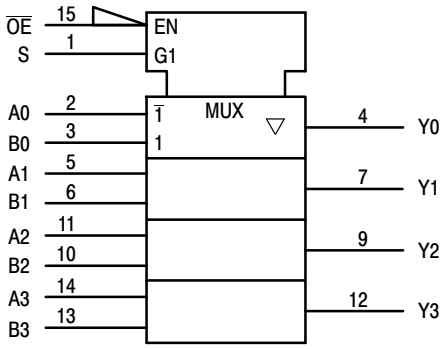


Figure 3. IEC Logic Symbol

FUNCTION TABLE

Inputs		Outputs
$\overline{OE}$	S	Y0 − Y3
H	X	Z
L	L	A0−A3
L	H	B0−B3

A0 − A3, B0 − B3 = the levels of the respective Data−Word Inputs.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 >2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	±300	mA
θ_{JA}	Thermal Resistance, Junction−to−Ambient	SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1 Tested to EIA/JESD22−A114−A
2 Tested to EIA/JESD22−A115−A
3 Tested to JESD22−C101−A
4 Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		−55	125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

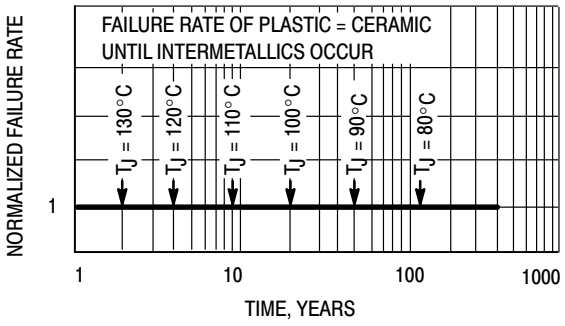


Figure 4. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55°C \le T_A \le 125°C$ Min	$-55°C \le T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 to 5.5	1.5 V_{CCX} 0.7			1.5 V_{CCX} 0.7	1.5 V_{CCX} 0.7	1.5 V_{CCX} 0.7		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 to 5.5			0.5 V_{CCX} 0.3		0.5 V_{CCX} 0.3		0.5 V_{CCX} 0.3	V
V_{OH}	Maximum High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.8		2.34 3.66		
V_{OL}	Maximum Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = 4 mA I_{OH} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	5.5			±0.25		±2.5		±2.5	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_{IN} = V_{CC} or GND	5.5			4.0		40.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A = \le 85°C$ Min	$T_A = \le 85°C$ Max	$-55°C \le T_A \le 125°C$ Min	$-55°C \le T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay A or B to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		5.8	9.3	1.0	11.0	1.0	11.0	ns
		V_{CC} = 3.3 ± 0.3 V C_L = 50 pF		8.3	12.8	1.0	14.5	1.0	14.5	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		3.6	5.9	1.0	7.0	1.0	7.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF		5.1	7.9	1.0	9.0	1.0	9.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay S to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		7.0	11.0	1.0	13.0	1.0	13.0	ns
		V_{CC} = 3.3 ± 0.3 V C_L = 50 pF		9.5	14.5	1.0	16.5	1.0	16.5	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		4.0	6.8	1.0	8.0	1.0	8.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF		5.5	8.8	1.0	10.0	1.0	10.0	
t_{PZL}, t_{PZH}	Maximum Output Enable Time $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF R_L = 1 kΩ		6.7	10.5	1.0	12.5	1.0	12.5	ns
		V_{CC} = 3.3 ± 0.3 V C_L = 50 pF R_L = 1 kΩ		9.2	14.0	1.0	16.0	1.0	16.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF R_L = 1 kΩ		3.6	6.8	1.0	8.0	1.0	8.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF R_L = 1 kΩ		5.1	8.8	1.0	10.0	1.0	10.0	
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF R_L = 1 kΩ		12.0	15.0	1.0	16.0	1.0	17.5	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF R_L = 1 kΩ		5.7	13.0	1.0	14.0	1.0	15.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 5)	20	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Characteristic	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.3	− 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

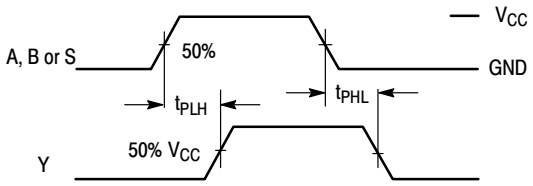


Figure 5. Switching Waveform

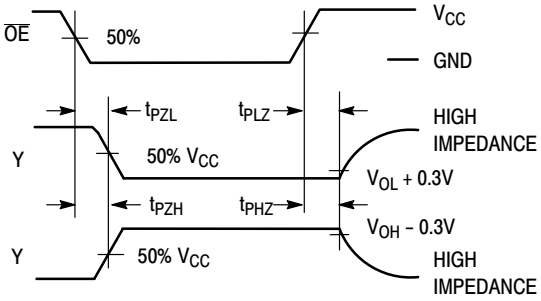
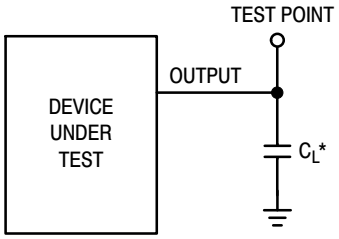
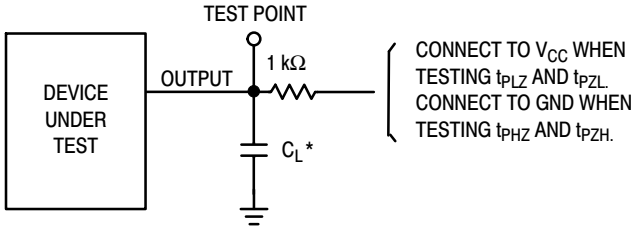


Figure 6. Switching Waveform



*Includes all probe and jig capacitance

Figure 7. Test Circuit



*Includes all probe and jig capacitance

Figure 8. Test Circuit

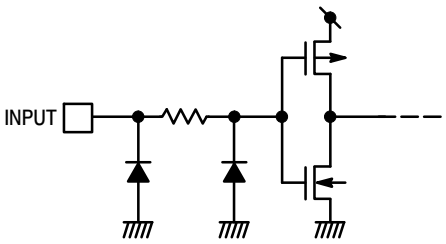
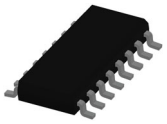


Figure 9. Input Equivalent Circuit

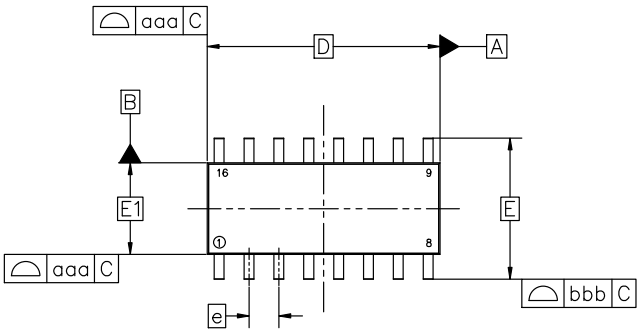
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



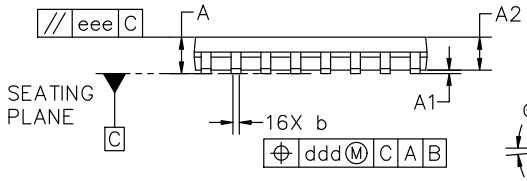
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

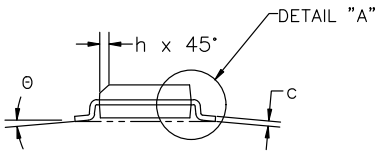
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

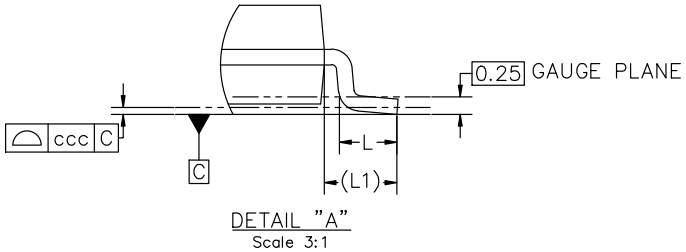


SIDE VIEW

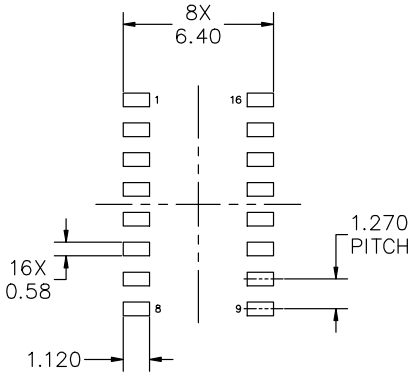


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

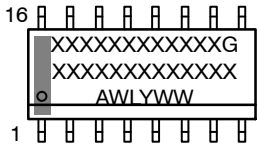
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

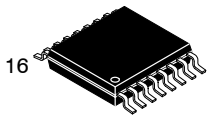
STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

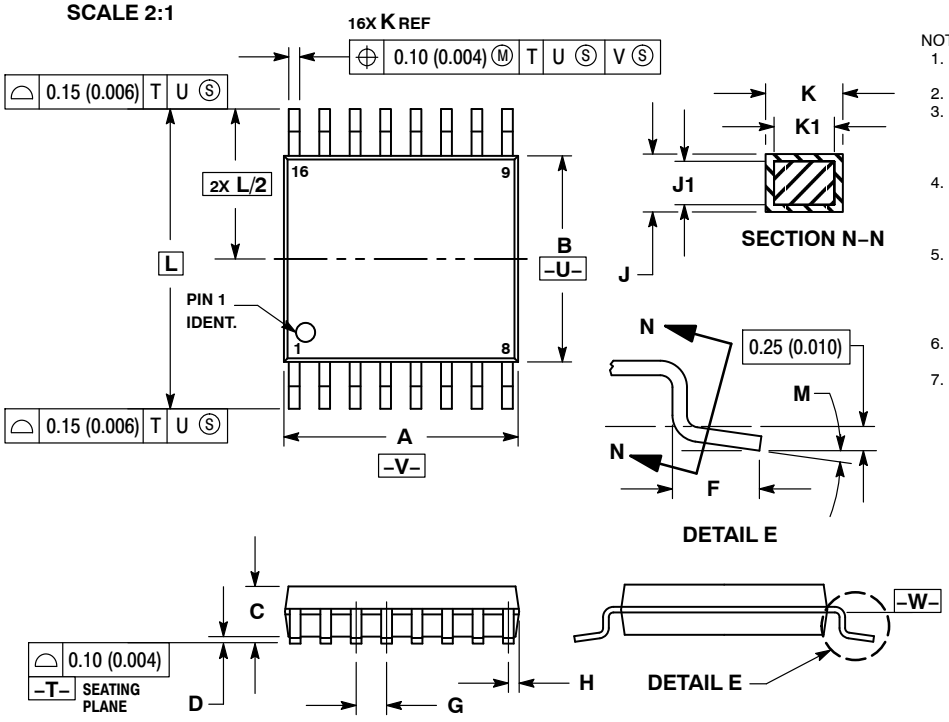
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006



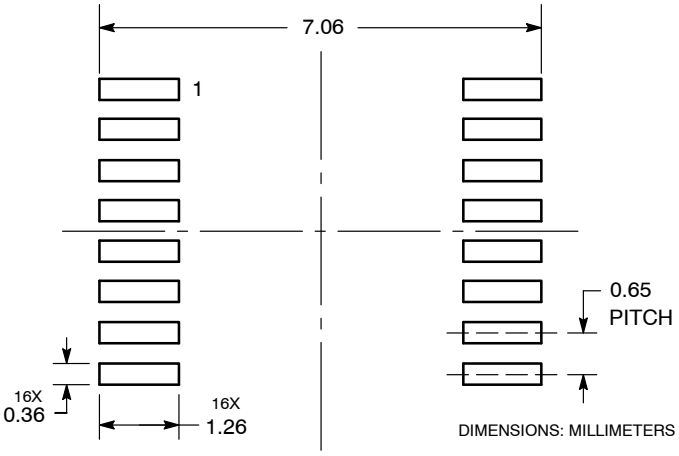
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

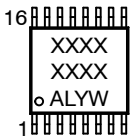
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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